IS32SE5118A

8-CH PROGRAMMABLE CAPACITIVE TOUCH SENSOR

GENERAL DESCRIPTION

IS32SE5118A is an ultra-low power, 8-channel capacitive touch controller. The controller allows sleep mode and uses auto-detection for wakeup. It also provides a shield output to increase moisture immunity. The built-in hardware monitor and calibration for the environment feature is to prevent false triggers.

A host MCU is required to communicate with IS32SE5118A. An on-chip I²C slave controller with 400kHz capability serves as the communication port for the host MCU. An interrupt, INT, can be configured and it is generated when a touch trigger event occurs. Trigger conditions can be configured by setting the interrupt register. IS32SE5118A can support proximity sensing.

IS32SE5118A is available in TSSOP-16 and wettable flank QFN-16 package. It operates from 2.35V to 5.5V over the temperature range from -40°C to +125°C.

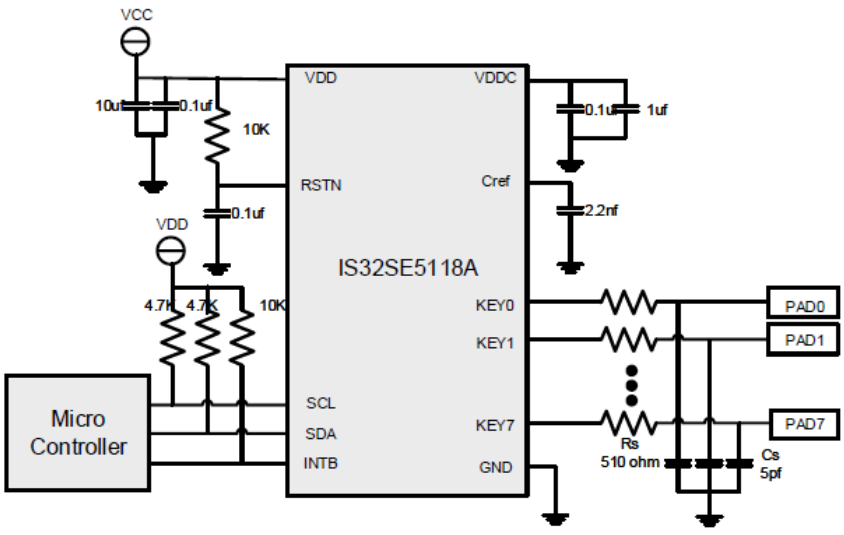
APPLICATIONS

- Touch keys for home appliances
- Touch keys for industrial control

FEATURES

- 8-channel capacitive touch controller with readable key value
- Touch threshold setting for individual key
- Optional multiple-key function
- Individual key calibration
- Interrupt output with auto-clear and repeating
- Auto sleep mode for extremely low power
- Keys wake up from sleep mode
- Buzzer/Melody Generator
- 400kHz fast-mode I²C interface
- Operating temperature between -40°C to +125°C
- TSSOP-16 and wettable flank QFN-16 (WQFN-16) package
- ROHS & Halogen-Free compliant package
- AEC-Q100 qualification
- TSCA compliance

TYPICAL APPLICATION CIRCUIT (TSSOP-16)



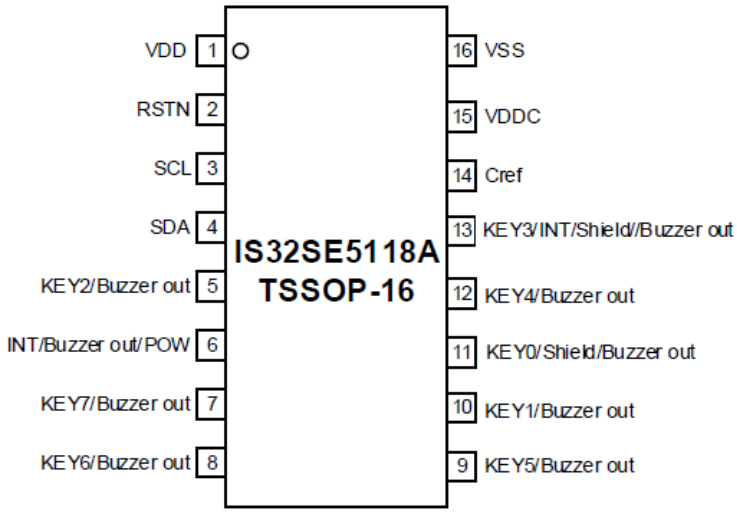
Note 1: SE5118A should be placed far away from the noise source for EMS.

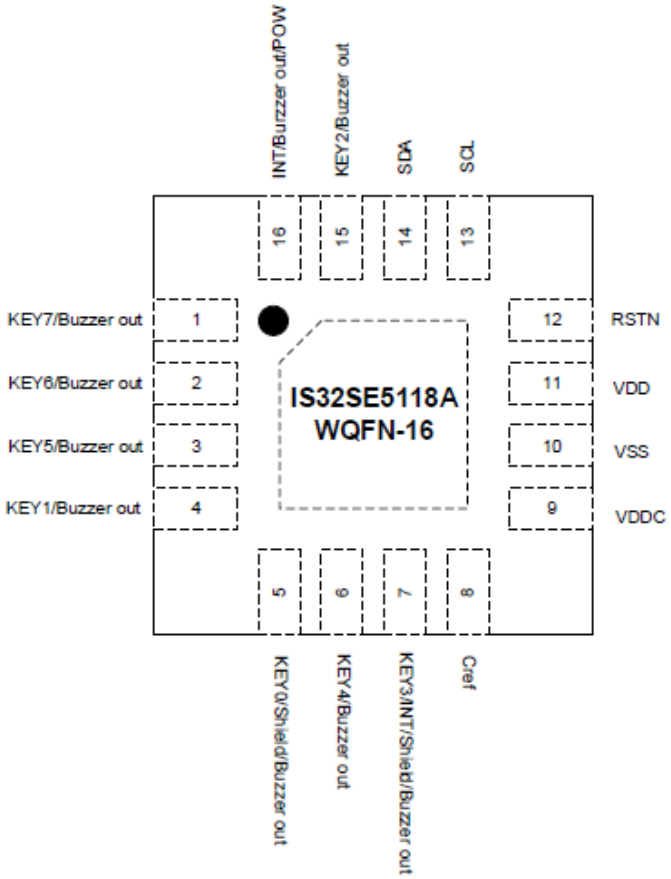
Note 2: R_S and C_S should be placed as close to the chip as possible to reduce EMI.

Note 3: INT can be configured as a POW pin for melody application.

Note 4: The capacitors connected to VDD and VDDC should be as close to the chip as possible to reduce EMI.

PINOUT


VDD 1
RSTN 2
SCL 3
SDA 4
KEY2/Buzzer out 5
INT/Buzzer out/POW 6
KEY7/Buzzer out 7
KEY6/Buzzer out 8
16 VSS
15 VDDC
14 Cref
13 KEY3/INT/Shield/Buzzer out
12 KEY4/Buzzer out
11 KEY0/Shield/Buzzer out
10 KEY1/Buzzer out
9 KEY5/Buzzer out
IS32SE5118A
TSSOP-16


INT/Burzzer out/POW
KEY2/Buzzer out
SDA
SCL
16
15
14
13
KEY7/Buzzer out 1
KEY6/Buzzer out 2
KEY5/Buzzer out 3
KEY1/Buzzer out 4
12 RSTN
11 VDD
10 VSS
9 VDDC
IS32SE5118A
WQFN-16
5
6
7
8
KEY0/Shield/Buzzer out
KEY4/Buzzer out
KEY3/INT/Shield/Buzzer out
Cref

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1. PIN DESCRIPTION

TSSOP-16	WQFN-16	NAME	PIN DESCRIPTION
1	11	VDD	Power supply
2	12	RSTN	Reset Low Active
3	13	SCL	I2C serial clock
4	14	SDA	I2C serial data
5	15	KEY2/Buzzer out	Multiple function pin. Can be configured to touch sense channel 2 or Buzzer output.
6	16	INT/Buzzer out/ POW	Multiple function pin. Can be configured to interrupt output (active low), Buzzer output, or melody power control (POW).
7 – 10	1 – 4	KEY7/6/5/1/ Buzzer out	Multiple function pins. Can be configured to Input sensor channel (refer to the PINOUT) or Buzzer output.
11	5	KEY0/Shield/ Buzzer out	Multiple function pin. Can be configured to Input sense channel 0, Shield output, or Buzzer output.
12	6	KEY4/Buzzer out	Multiple function pin. Can be configured to Input sense channel 4 or Buzzer output.
13	7	KEY3/INT/ Shield/ Buzzer out	Multiple function pin. Can be configured to Input sense channel 3, interrupt output (active low), Shield output, or Buzzer output.
14	8	Cref	External reference Capacitor for touch sense
15	9	VDDC	Internal 1.5V power supply. Connect to external 1.0uF decoupling capacitor.
16	10	VSS	Ground

Table 1-1 PIN Description

2. ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY
IS32SE5118A-ZNLS3-TR	TSSOP-16, Lead-free	2500/Reel
IS31SE5118A-QFLS3-TR	WQFN-16, Lead-free	2500/Reel

3. ABSOLUTE MAXIMUM RATINGS

Supply voltage, VDD	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ V_{DD}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range TA	-40°C ~ +125°C
Junction Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	50.2°C/W(TSSOP-16) 53.5°C/W(WQFN-16)
ESD (HBM) ESD (CDM)	±2kV ±750V

Table 3-1 Absolute maximum ratings

Note 3: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.1 ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = 2.35V ~ 5.5V, unless otherwise noted. Typical values are T_A = 25°C, V_{DD} = 3.6V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		2.35		5.5	V
I_{DD}	Quiescent power supply current	V_{DD} = 5.5V		50		μA
ΔC_S	Minimum detectable capacitance	C_S = 5pF (Note 4)		0.2		pF
Logic Electrical Characteristics						
V_{IL}	Logic “0” input voltage	V_{DD} = 2.7V			0.4	V
V_{IH}	Logic “1” input voltage	V_{DD} = 5.5V	1.4			V
I_{IL}	Logic “0” input current	V_{INPUT} = 0V (Note 4)		5		nA
I_{IH}	Logic “1” input current	V_{INPUT} = V_{DD} (Note 4)		5		nA

3.2 DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 4)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{SCL}	Serial-Clock frequency				400	kHz
t_{BUF}	Bus free time between a STOP and a START condition		1.3			μs
$t_{HD, STA}$	Hold time (repeated) START condition		0.6			μs
$t_{SU, STA}$	Repeated START condition setup time		0.6			μs
$t_{SU, STO}$	STOP condition setup time		0.6			μs
$t_{HD, DAT}$	Data hold time				0.9	μs
$t_{SU, DAT}$	Data setup time		100			ns
t_{LOW}	SCL clock low period		1.3			μs
t_{HIGH}	SCL clock high period		0.7			μs
t_R	Rise time of both SDA and SCL signals	(Note 5)		20+0.1C_b	300	ns
t_F	Fall time of both SDA and SCL signals	(Note 5)		20+0.1C_b	300	ns

Note 4: Guaranteed by design.

Note 5: Cb = total capacitance of one bus line in pF. ISINK ≤ 6mA. tR and tF measured between 0.3 × VDD and 0.7 × VDD.

4. FUNCTION BLOCK DIAGRAM

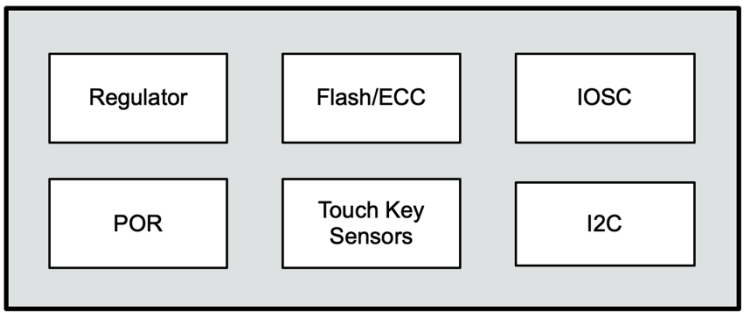


Figure 4-1 Functional Block Diagram

4.1 Basic introduction for touch sense data process flow

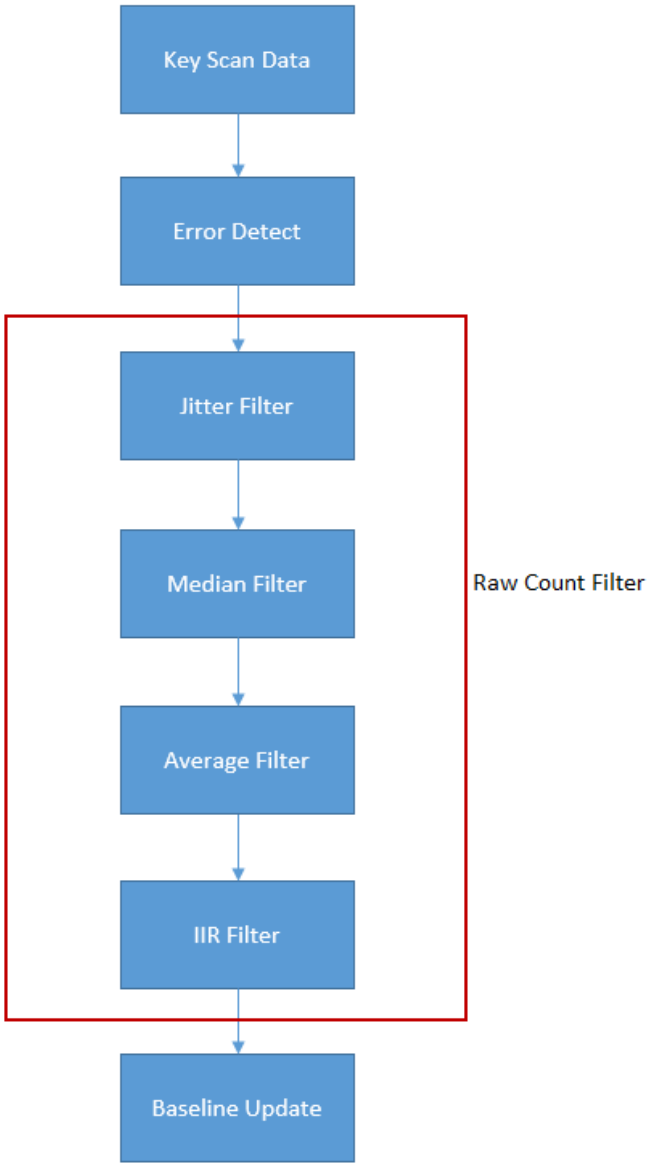


Figure 4-2 Touch Sense Data Process Flow

Baseline will be updated to the current raw count based on the below factors. For detailed information about baseline, please refer to Section 4.4.2 Key parameter in “IS31SE5118A Eval Board User's Manual” application note.

4.1.1 Positive noise threshold

Baseline is updated if the difference count of baseline count and raw count is below the positive noise threshold.

4.1.2 Negative noise threshold

It is used with the low baseline reset count to reset baseline count to the current raw count. Please refer to the description of Low baseline reset.

4.1.3 Low baseline reset

Low baseline reset count of each key. A reset count increases one if the absolute |raw count – baseline| > negative noise threshold. Once the reset count exceeds the low baseline reset register value, the baseline is reset to the current raw count. The reset count will be reset to 0 if the absolute | raw count – baseline| <= negative noise threshold.

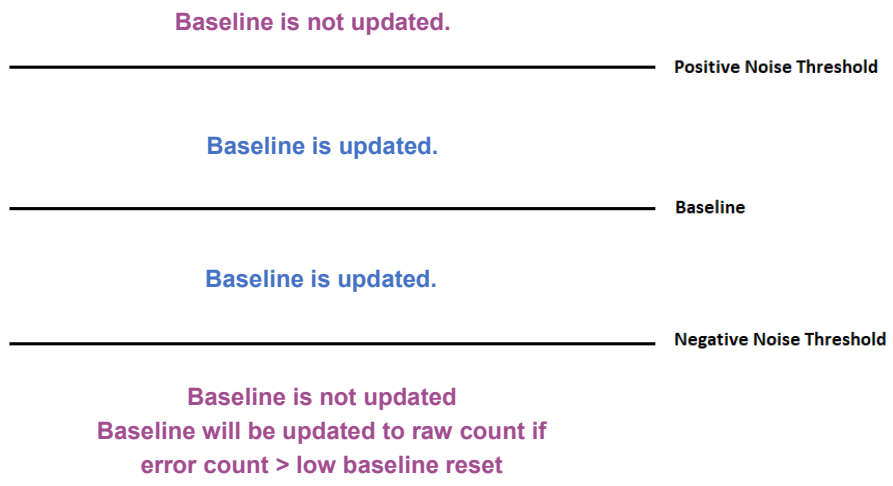


Figure 4-3 Baseline Process based on difference of baseline and raw count

4.1.4 Touch sense data identification

Ignore touch key scan if the signal exceeds the lock threshold.

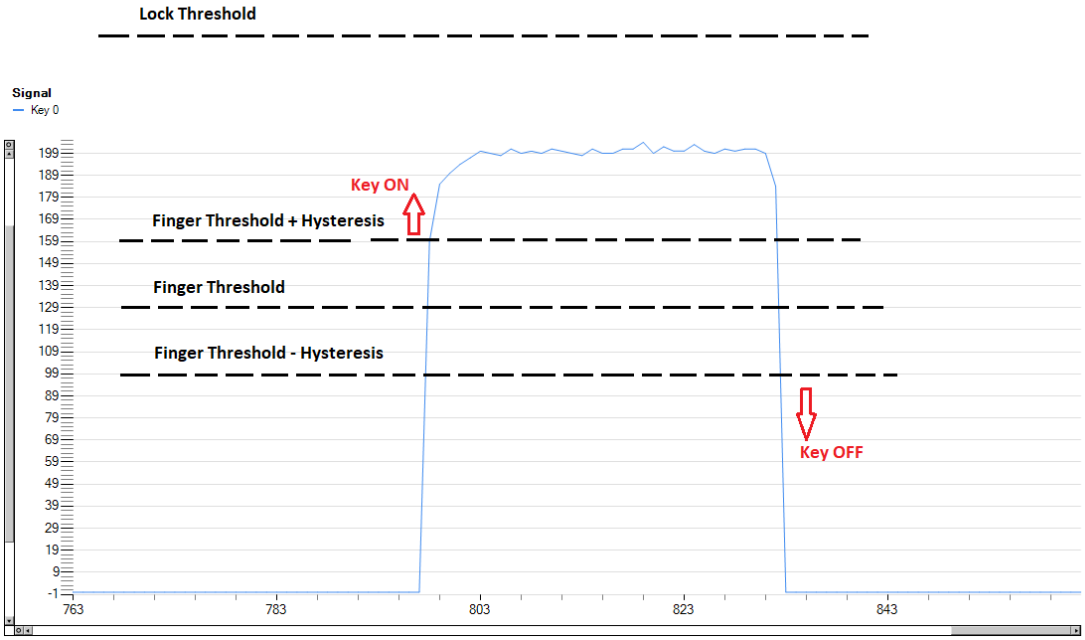


Figure 4-4 Touch Sense Data Identification

5. DETAILED DESCRIPTION

5.1 I2C INTERFACE

IS32SE5118A uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. IS32SE5118A has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 "0" for a write command and set A0 "1" for a read command.

The complete slave address is:

Bit	A7:A1	A0
Value	0111100	1/0

The SCL line is uni-directional. The SDA line is bi-directional (open collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. During communication, the microcontroller is the master and IS32SE5118A is the slave.

The timing diagram for the I2C is shown in Figure 5-1. The SDA is latched on to the stable high level of the SCL. When there is no bus activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next and most significant bit first. Each address bit must be ready while the SCL level is high.

After the last bit of the chip address is sent, the master checks for IS32SE5118A's acknowledge. The master releases the SDA line high (through a pull-up resistor). and sends an SCL pulse. If IS32SE5118A has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS32SE5118A, the register address byte is sent and most significant bit first. IS32SE5118A must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, and most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, IS32SE5118A must generate another acknowledgement to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

5.2 READING PORT REGISTERS

To read the device data, the bus master must first send the address of IS32SE5118A with the R/$\overline{W}$ bit set to "0", followed by the register address byte, which determines which register is accessed. After a restart, the bus master must send IS32SE5118A address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is sent from IS32SE5118A to the master (Figure 5-4).

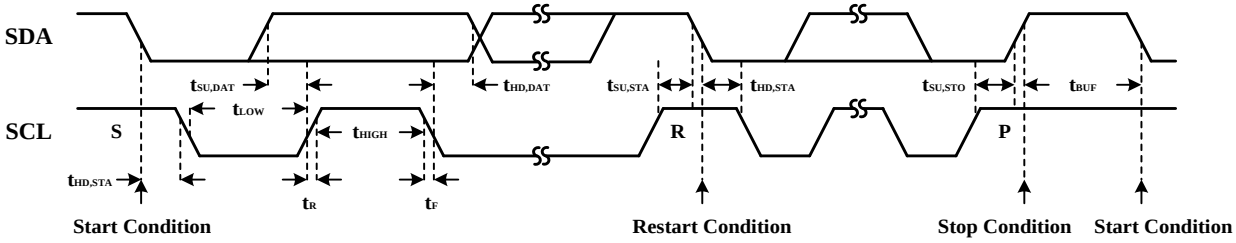


Figure 5-1 Interface Timing

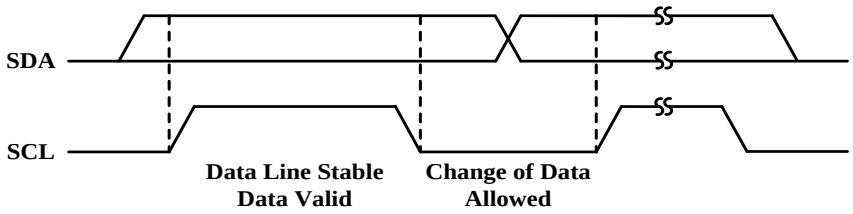


Figure 5-2 Bit Transfer

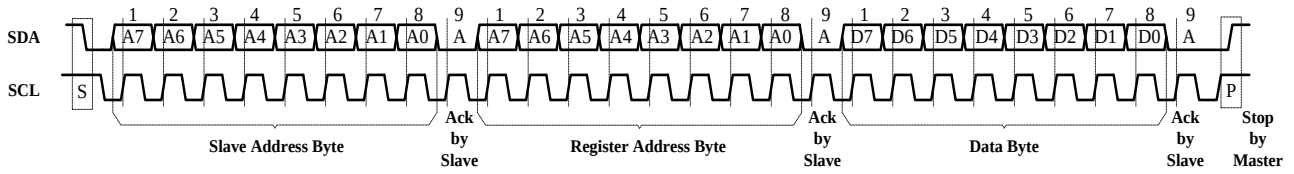


Figure 5-3 Writing to IS32SE5118A

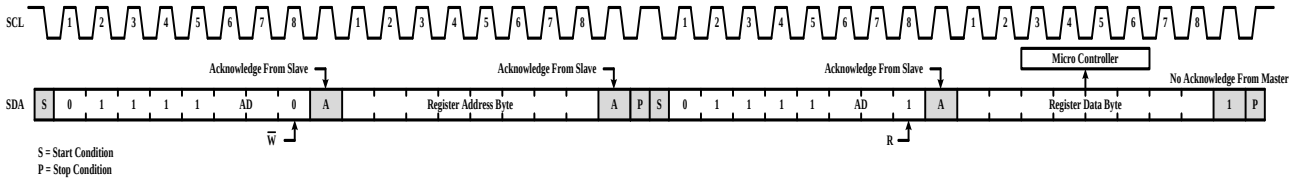


Figure 5-4 Reading from IS32SE5118A

Note: Successive read or write protocol is supported.

6. REGISTER DEFINITION

Address	Name	Definition	R/W	Default
00h	Chip Part Number	Chip's part number	R	18h
01h-02h	Chip Version	Chip's version	R	-
03h	Firmware Version	Firmware version	R	60h
04h	Run Version	Run version	R/W	60h
05h	Main Control	System reset, power saving, and parameters management	W	00h
06h	-	Reserved	-	-
07h	Key Status	Key 0-Key 7 status bits	R	00h
08h	Buzzer W	Buzzer data or stop command	W	-
08h	Buzzer R	Available buzzer buffer size	R	0Ah
09h-10h	Key Signal	Key 0-Key 7 signal value	R	00h
11h-20h	Key Raw Count	Key 0-Key 7 raw count value	R	0000h
21h-30h	Key Baseline	Key 0-Key 7 baseline value	R	0000h
31h-38h	Key Finger Threshold	Key 0-Key 7 finger threshold setting	R/W	50h
39h-40h	Key Noise Threshold	Key 0-Key 7 noise threshold setting	R/W	28h
41h-48h	Key Negative Noise Threshold	Key 0-Key 7 negative noise threshold setting	R/W	28h
49h-50h	Key Low Baseline Reset	Key 0-Key 7 low baseline reset setting	R/W	1Eh
51h-58h	Key Hysteresis	Key 0-Key 7 hysteresis setting	R/W	0Ah
59h-60h	Key ON Debounce	Key 0-Key 7 de-bounce setting	R/W	02h
61h	Key Interrupt Enable	Key 0-Key 7 enable Interrupts associated with capacitive touch sensor inputs	R/W	00h
62h-69h	Reserved	-	-	-
6Ah-71h	Reserved	-	-	-
72h	Raw Count Filter	Raw count filter setting	R/W	00h
73h	Baseline IIR Ratio	Baseline IIR ratio setting	R/W	01h
74h	Lock Threshold High Byte	Lock threshold High Byte setting	R/W	03h
75h	Lock Threshold Low Byte	Lock threshold Low Byte setting	R/W	E8h
76h	Lock Scan Cycle	Lock scan cycle setting	R/W	08h
77h	Raw Count Difference Limit	Raw count difference limit setting	R/W	64h
78h	Multi Touch Key Configure	Multiple touch key function setting	R/W	01h
79h	Max Duration Time	Maximum duration time setting	R/W	1Ah
7Ah	Interrupt Configuration	Interrupt configuration	R/	0Ah
7Bh	Interrupt Repeat Time	Repeat cycle for pressing key interrupt setting	R/W	00h
7Ch	Key Pin Select	Select pins as Key0-Key7	R/W	00h
7Dh	Shield Pin Select	Select pin as shield	R/W	08h
7Eh-7Fh	INT Pin Select	Select pin as INT	R/W	0000h
80h	Buzzer Pin Select	Select pin as buzzer for Key0-Key7	R/W	04h
81h	Buzzer Pin Select	Select pin as buzzer for Pin 13	R/W	00h
82h	Buzzer Power Pin Select	Select pin as buzzer power for Key0-Key7	R/W	00h
83h	Buzzer Power Pin Select	Select pin as buzzer power for Pin 13	R/W	01h

Address	Name	Definition	R/W	Default
84h	TKIII Control 1	Repeat sequence, discard starting edges, inserts an inter-sequence idle time, and low-frequency noise filter	R/W	13h
85h	TKIII Control 2	Pseudo random sequence setting	R/W	20h
86h	TKIII Control 3	Multi frequency scan/cycle count setting	R/W	03h
87h	TKIII CCHG	Internal charge capacitance setting	R/W	60h
88h	TKIII PUD	Pull-up current/ pull-up resistors setting	R/W	00h
89h	System Clock Select	System clock setting	R/W	01h
8Ah	Spread Spectrum	Spread spectrum setting	R/W	0Ch
8Bh	Auto Sleep Mode	Auto-enter sleep mode time setting	R/W	0Fh
8Ch	Sleep Mode Control	Sleep mode control setting	R/W	00h
8Dh	Wake Up Key Select	Select Key0~Key7 to exit sleep mode	R/W	00h
8Eh	Wake Up Threshold	Wake up threshold setting	R/W	08h
8Fh	TKIII Sleep Mode CCHG	Sleep mode internal charge capacitance setting	R/W	60h
90h	TKIII Sleep Mode PUD	Sleep mode pull-up current/ pull-up resistors setting	R/W	00h
91h-92h	Sleep Mode Raw Count	Sleep mode raw count value	R	0000h
93h-94h	Sleep Mode Baseline	Sleep mode baseline value	R	0000h
95h	Key Scan Once	I2C control key scan	R/W	00h
96h	Table Ready Mark	Mark for flash data ready	R	00h

Table 6-1 Page 0 Register list

00h Chip Part Number Register (RO)

Bit	D7:D0
Name	CPN[7:0]
Default	0001 1000

CPN Chip Part Number
Chip's part number 18h

01h Chip Version Register 1 (RO)

Bit	D7:D0
Name	CV1[7:0]
Default	-

CV1 Chip Version **information 1**

02h Chip Version Register 2 (RO)

Bit	D7:D0
Name	CV2[7:0]
Default	-

CV2 Chip Version **information 2**
CV1 & CV2 bytes contain chip revision. CV1 indicates mask set version. CV2 indicates minor version.

03h Firmware Version Register (RO)

Bit	D7:D0		
Name	FV1[2:0]	FV2[2:0]	FV3[1:0]
Default	010	000	00

FV Firmware Version
Default version is 2.0.0
FV1[2:0] Major version
FV2[2:0] Minor version
FV3[1:0] Patch version

04h Run Version Register (RW)

Bit	D7:D0		
Name	RV1[2:0]	RV2[2:0]	RV3[1:0]
Default	011	000	00

RV Run Version
Set run firmware version and the default value equals to the default value of the firmware version register
RV1[2:0] Major version
RV2[2:0] Minor version
RV3[1:0] Patch version

05h Main Control Register (WO)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SR	RD	-	SP	SS	DW	DS	-
Default	0	0	0	0	0	0	0	0

SR System Reset
1 System reset
RD Reset All Parameters to Manufacturer Default Setting.
1 Reset all user-defined parameters to manufacture default setting.
SP Sleep Mode
1 Sleep mode
SS Save User-Defined Parameters
1 Save current parameters into flash.
DW Deep Sleep Wake Up Reset Baseline
1 Reset touch key baseline after waking up from deep sleep mode.
DS Deep Sleep Mode
1 Keep sleep until waking up by I2C SDA falling edge.

06h Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

Reserved

07h Key Status Register (RO)

Bit	D7:D0
Name	KS[7:0]
Default	0000 0000

KSx Key0~Key7 Status
If the key is detected as pressed, the corresponding bit (KSx) will be set to “1”.
0 Not detected.
1 Key is detected.

08h Buzzer Register (W)

Bit	D7:D0
Name	BW[7:0]
Default	-

BW Buzzer Register Write
Buzzer data or stop command

08h Buzzer Register (R)

Bit	D7:D0
Name	BR[7:0]
Default	0000 1010

BR — Buzzer Register Read
It shows the available tone buffer size. SE5118A has 10 built-in note buffers.

09h~10h KEY0~KEY7 Signal Register (RO)

Bit	D7:D0
Name	KEYx_SIGNAL[7:0]
Default	0000 0000

KEYx_SIGNAL — Key Signal Count
The difference between baseline and raw count.

The maximum value is 254. It will keep 254 if the value is over 254. Value 255 means noise existence.

11h, 13h …, 1Dh, 1Fh KEY0~KEY7 Raw Count High Byte Register (RO)

Bit	D7:D0
Name	KEYx_RAWCOUNT[15:8]
Default	0000 0000

12h, 14h …, 1Eh, 20h KEY0~KEY7 Raw Count Low Byte Register (RO)

Bit	D7:D0
Name	KEYx_RAWCOUNT[7:0]
Default	0000 0000

KEYx_RAWCOUNT — Raw count of each key, provides an indication of the magnitude of the sensor's capacitance.

21h, 23h …, 2Dh, 2Fh KEY0~KEY7 Baseline High Byte Register (RO)

Bit	D7:D0
Name	KEYx_BASELINE[15:8]
Default	0000 0000

22h, 24h …, 2Eh, 30h KEY0~KEY7 Baseline Low Byte Register (RO)

Bit	D7:D0
Name	KEYx_BASELINE[7:0]
Default	0000 0000

KEYx_Baseline — Baseline of each key

31h~38h KEY0~KEY7 Finger Threshold Register (RW)

Bit	D7:D0
Name	KEYx_TH[7:0]
Default	0101 0000

KEYx_TH — Finger threshold of each key. It is used with hysteresis to determine the key state.

39h~40h KEY0~KEY7 Noise Threshold Register (RW)

Bit	D7:D0
Name	KEYx_NTH[7:0]
Default	0010 1000

KEYx_NTH — Noise threshold of each key
Baseline needs to be updated if the difference (baseline and raw count) is less than the noise threshold.

41h~48h KEY0~KEY7 Negative Noise Threshold Register (RW)

Bit	D7:D0
Name	KEYx_NNTH[7:0]
Default	0010 1000

KEYx_NNTH Negative noise threshold of each key

49h~50h KEY0~KEY7 Low Baseline Reset Register (RW)

Bit	D7:D0
Name	RCx[7:0]
Default	0001 1110

RCx Reset Count

Low baseline reset count of each key. A reset count increases one if the absolute |raw count – baseline| > absolute |negative noise threshold|. Once the reset count exceeds the low baseline register value, the baseline is reset to the current raw count. The reset count will be reset to 0 if the absolute |raw count – baseline| <= absolute |negative noise threshold|.

51h~58h KEY0~KEY7 Hysteresis Register (RW)

Bit	D7:D0
Name	HYSTERESISx[7:0]
Default	0000 1010

HYSTERESISx Hysteresis of each key

59h~60h KEY0~KEY7 On Debounce Register (RW)

Bit	D7:D0
Name	DEBOUNCEx[7:0]
Default	0000 0010

DEBOUNCEx De-bounce number of each key. When the acquired number > de-bounce setting value, then the key is granted as on.

61h Key Interrupt Enable Register (RW)

Bit	D7:D0
Name	INTEN[7:0]
Default	0000 0000

The Interrupt Enable Register determines whether a key is detected and it causes the interrupt pin to be asserted.

INTEN Key Interrupt Enable
0 Disable
1 Enable

The default value for Interrupt Enable Registers is interrupt disable. Setting INE bit of Interrupt Configuration Register (69h) to “1”, INT pin will generate interrupt signal.

62h~69h Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	-
Default	-	-	-	-	-	-	-	-

Reserved

6Ah~71h Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	-
Default	-	-	-	-	-	-	-	-

Reserved

72h Raw Count Filter Register (RW)

Bit	D7	D6	D5:D4	D3	D2:D1	D0
Name	MF	AF	IIR[1:0]	JF	JD[1:0]	-
Default	0	0	00	0	00	0

MF Median Filter
0 Disable
1 Enable

AF Average Filter
0 Disable
1 Enable

IIR IIR Filter
00 Disable
01 1/2
10 1/4
11 1/8

JF Jitter Filter
0 Disable
1 Enable

JD Jitter Delta
00 1
01 2
10 4
11 8

73h Baseline IIR Ratio Register (RW)

Bit	D7:D0
Name	RATIO[7:0]
Default	0000 0001

RATIO Range 1 ~ 255

74h Lock Threshold High Byte Register (RW)

Bit	D7:D0
Name	LT[15:8]
Default	0000 0011

75h Lock Threshold Low Byte Register (RW)

Bit	D7:D0
Name	LT[7:0]
Default	1110 1000

LT Lock Threshold

76h Lock Scan Cycle Register (RW)

Bit	D7:D0
Name	LSC[7:0]
Default	0000 1000

LSC Lock Scan Cycle
Ignore the key scan data for the setting Lock scan cycle if the |raw count – baseline| > Lock threshold.

77h Raw Count Difference Limit Register (RW)

Bit	D7:D0
Name	RCDL[7:0]
Default	0110 0100

RCDL Raw Count Difference Limit
Ignore the key scan data if the difference between previous raw count and current raw count exceeds the limit.

78h Multiple Touch Key Configure Register (RW)

Bit	D7:D2	D1:D0
Name	-	MTK[1:0]
Default	000000	01

MTK Multi Touch Key
00 Allow all keys to be triggered at one time.
01 Allow one key to be triggered at one time.
10 Allow two keys to be triggered at one time.
11 Allow three keys to be triggered at one time.

79h Max Duration Time Register (RW)

Bit	D7	D6	D5	D4	D3:D0
Name	-	-	-	MDEN	MDT[3:0]-
Default	0	0	0	1	1010

MDEN Maximum Duration Time Enable
0 Disable
1 Enable

MDT Maximum Duration Time
0000 0.5s
0001 1s
0010 2s
0011 3s
0100 4s
0101 5s
0110 6s
0111 7s
1000 8s
1001 9s
1010 10s
1011 11s
1100 12s
1101 13s
1110 14s
1111 15s

MDT bits set the pressed time. When the key pressed duration exceeds the programmed time (MDT), the device will be forced to calibrate the pressed key. Set MDEN to “1” will enable this function.

7Ah Interrupt Configuration Register (RW)

Bit	D7	D6:D4	D3	D2:D0
Name	INE	-	ACEN	ACT[2:0]
Default	0	000	1	010

INE Interrupt Function Enable
0 Disable
1 Enable

ACEN Auto-Clear Interrupt Enable
0 Disable
1 Enable

ACT Auto-Clear Interrupt Time
000 10ms
001 20ms
010 30ms
011 40ms

100 50ms
101 100ms
110 150ms
111 200ms

When ACEN=0, the INT will keep low until the device 07h register is read, or the key is released. When ACEN=1, the INT will be released after ACT setting time is expired even 07h register is not read, or key is still pressed.

7Bh Interrupt Repeat Time Register (RW)

Bit	D7:D4	D3:D0
Name	-	INTRT[3:0]
Default	0000	0000

INTRT Interrupt Repeat Time
0000 disable
0001 50ms
0010 100ms
0011 150ms
0100 200ms
0101 250ms
0110 300ms
0111 350ms
1000 400ms
1001 450ms
1010 500ms
1011 600ms
1100 700ms
1101 800ms
1110 900ms
1111 1s

After INTRT is set, a second interrupt will be generated after the interrupt repeat time is expired If there is a key keeping pressed.

7Ch Key Pin Select Register (RW)

Bit	D7:D0
Name	KS[7:0]
Default	0000 0000

KS Key Pin Selection Setting
0 Disable
1 Enable

7Dh Shield Pin Select Register (RW)

Bit	D7:D0
Name	SHDE[7:0]
Default	0000 1000

SHDE Shield Enable (only for bit0 and bit3)
0 Disable shield driver
1 Enable shield driver

7Eh INT Pin Select Register 1 (RW)

Bit	D7:D0
Name	IPS1[7:0]
Default	0000 0000

7Fh INT Pin Select Register 2 (RW)

Bit	D0
Name	IPS2[0]
Default	0

IPS1/2 INT Pin Select 1/2
IPS1[7:0] maps to KEY[7:0]. Write 1 will enable the related Key as an INT pin.
IPS2[0] maps to Pin 13. Write 1 will enable Pin13 as an INT pin.

80h Buzzer Pin Select Register 1 (RW)

Bit	D7:D0
Name	BPS1[7:0]
Default	0000 0100

81h Buzzer Pin Select Register 2 (RW)

Bit	D0
Name	BPS2[0]
Default	0

BPS1/2 Buzzer output Select 1/2
BPS1[7:0] maps to KEY[7:0]. Write 1 will enable the related Key as a Buzzer output pin.
BPS2[0] maps to Pin 13. Write 1 will enable Pin 13 as a Buzzer output pin.

82h Buzzer Power Pin Select Register 1 (RW)

Bit	D7:D0
Name	EBP1[7:0]
Default	0000 0000

83h Buzzer Power Pin Select Register 2 (RW)

Bit	D0
Name	EBP2[0]
Default	1

EBP1/2 Buzzer Power Select 1/2
EBP1[7:0] maps to KEY[7:0]. Write 1 will enable the related Key as a Buzzer Power pin.
EBP2[0] maps to Pin 13. Write 1 will enable Pin 13 as a Buzzer Power pin.

84h TKIII Control Register 1 (RW)

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	RPT	INI	ASTDLY	
Default	00	01	00	11

RPT Repeat Sequence Count
00 No repeat
01 Repeat 4 times
10 Repeat 8 times
11 Repeat 16 times

INI Initial Setting Delay
INI[1-0] defines the number of TKCLK periods for the initial settling of pin Cref. The delay is (INI[1-0] + 1) *4*TKCLK.

ASTDLY Auto Mode Start Delay
ASTDLY[1-0] inserts an inter-sequence idle time of (ASTDLY[1-0] +1) * 256 TKCLK at each sequence start. This delay allows the stabilization time from normal mode to sleep mode.

LFNF Low-Frequency Noise Filter Setting
00 disable LFNE

If the scan count with noise injection detection is larger than (LFNF[1-0] * 8), the scan result is ignored.

85h TKIII Control Register 2 (RW)

Bit	D7	D6	D5	D4	D3	D2:D1	D0
Name	-	-	PRS	-	-	-	-
Default	0	0	1	0	0	00	0

PRS Pseudo Random Sequence
0 Disable PRS
1 Enable PRS

86h TKIII Control Register 3 (RW)

Bit	D7:D4	D3	D2:D0
Name	-	MFEN	CCNT[2:0]
Default	0000	0	011

MFEN Multi Frequency Scan
0 Disable MF
1 Enable MF

CCNT Cycle Count of Each Conversion Sequence
000 1024
001 2048
010 4096
011 8192
100 12288
101 16384
110 32768
111 65536

87h TKIII CCHG Register (RW)

Bit	D7:D5	D4:D0
Name	CCHG[2:0]	-
Default	011	00000

CCHG Internal Reference Capacitance Select
000 10pF
001 20pF
010 30pF
011 40pF
100 50pF
101 60pF
110 70pF
111 80pF

88h TKIII PUD Register (RW)

Bit	D7	D6	D5:D4	D3:D0
Name	PUDIEN	PUDREN	-	PUD[3:0]
Default	0	0	00	0000

TK3PUD is to configure a constant DC pull-up/pull-down on pin Cref to allow high capacitance touch-key detection. A DC pull-up/pull-down can compensate for the equivalent resistance which is caused by a high capacitance key. Connecting a constant current source or resistor can thus maintain touch key detection sensitivity. In general, we will try to maintain the raw count around half of CCNT for the case without key touched.

For DC current, PUD[3:0] enables 8uA/4uA/2uA/1uA current source. For Resistor, PUD[3-0] enables 5K/10K/20K/40K resistor.

PUDIEN Pull-up/Pull-down DC Current Enable
PUDREN Pull-up/Pull-down DC Resistor Enable
PUD Pull up DC Current

1000 Enable 8uA current source.
0100 Enable 4uA current source.
0010 Enable 2uA current source.
0001 Enable 1uA current source.

PUD Pull up Resistor
1000 Enable 5K resistor source.
0100 Enable 10K resistor source.
0010 Enable 20K resistor source.
0001 Enable 40K resistor source.

89h System Clock Select Register (RW)

Bit	D7:D4	D3	D2:D0
Name	SCS[3:0]-	CLKS	TKCS[2:0]
Default	0000	0	001

SCS System Clock Select
0000 16MHz / 1
0001 16MHz / 2
0010 16MHz / 4
0011 16MHz / 6
0100 16MHz / 8
0101 16MHz / 10
0110 16MHz / 12
0111 16MHz / 14
1000 16MHz / 16
1001 16MHz / 32
1010 16MHz / 64
1011 16MHz / 128
1100 16MHz / 256
1101 16MHz / 256
1110 16MHz / 256
1111 16MHz / 256

CLKS Clock Stretching (For I2C)
0 Disable stretching
1 Enable stretching

TKCS Touch Key Clock Select
000 System Clock / 2
001 System Clock / 4
010 System Clock / 6
011 System Clock / 8
100 System Clock / 10
101 System Clock / 16
110 System Clock / 32
111 64KHz

8Ah Spread Spectrum Register (RW)

Bit	D7:D2		
Name	SSR[3:0]	SSA[1:0]	-
Default	0000	11	-

SS Spread Spectrum Setting
With spread spectrum technique, electromagnetic energy produced over a particular bandwidth is spread in the frequency domain, and that can reduce EMI. Two parameters are listed as follows:

SSR[3:0] Defines the spread spectrum sweep rate. If the SSR[3:0] =0, then spread spectrum is disabled.

SSA[1:0] Defines how to adjust the spread spectrum frequency bandwidth. The frequency is adjusted by adding SSA [1:0] range to the actual internal OSC control register.

SSA[1:0]=11 +/- 32

SSA[1:0]=10 +/- 16
SSA[1:0]=01 +/- 8
SSA[1:0]=00 +/- 4

8Bh Auto Sleep Mode Register (RW)

Bit	D7	D6	D5:D4	D3:D0
Name	ASEN	-	BLMA[1:0]	AST[3:0]-
Default	0	0	00	1111

ASE N Auto-SLEEP Enable
0 Disable
1 Enable

BLMA Baseline moving average
Hardware baseline can be generated by slow moving average setting.
00 32 average
01 64 average
10 128 average
11 256 average

AST Auto Sleep Time
0000 0.5s
0001 1s
0010 1.5s
0011 2s
0100 2.5s
0101 3s
0110 3.5s
0111 4s
1000 4.5s
1001 5s
1010 6s
1011 7s
1100 8s
1101 9s
1110 10s
1111 11s

8Ch Sleep Mode Control Register (RW)

Bit	D7	D6	D5	D4	D3:D2	D1:D0
Name	-	PW	-	SC	T2[1:0]	T1[1:0]
Default	0	0	0	0	00	00

PW Proximity Wakeup
Disable: wake up>>scan key once>>go to sleep again
Enable: wake up>> generates INT signal (optional) >>go to sleep after Auto Sleep Time is expired if no key is detected
0 Disable
1 Enable

SC Sleep Calibration
0 Disable
1 Enable

T2 Wake Up Period with Key Disable
Device will be woken up according to the T2 setting by polling the status of Key.
00 50ms
01 100ms
10 200ms
11 300ms

T1 Wake Up Period with Key Enable
The device will be woken up according to the T1 setting to maintain the baseline to prevent the change of environment from stopping Key waking up the device.

00 2s
01 4s
10 8s
11 16s

8Dh Wake Up Key Select Register (RW)

Bit	D7:D0
Name	WK[7:0]
Default	0000 0000

WK Wakeup Key Select Setting
0 Disable
1 Enable

8Eh Wake Up Threshold Register (RW)

Bit	D7:D0
Name	WTH[7:0]
Default	0000 1000

Wake up threshold range from 0 to 255

8Fh TKIII Sleep Mode CCHG Register (RW)

Bit	D7:D5	D4:D0
Name	CCHG[2:0]	-
Default	011	00000

CCHG Internal Reference Capacitance Select
000 10pF
001 20pF
010 30pF
011 40pF
100 50pF
101 60pF
110 70pF
111 80pF

90h TKIII Sleep Mode PUD Register (RW)

Bit	D7	D6	D5:D4	D3:D0
Name	PUDIEN	PUDREN	-	PUD[3:0]
Default	0	0	00	0000

TK3 PUD is to configure a constant DC pull-up/pull-down on pin Cref to allow high capacitance touch-key detection. A DC pull-up/pull-down can compensate for the equivalent resistance caused by a high capacitance key. Connecting a switching current source or resistor can thus maintain touch key detection sensitivity.

For DC current, PUD[3:0] can enable 8uA/4uA/2uA/1uA current source. For Resistor, PUD[3-0] can enable 5K/10K/20K/40K resistor.

PUDIEN Pull-up/Pull-down DC Current Enable
PUDREN Pull-up/Pull-down DC Resistor Enable
PUD Pull up DC Current
1000 Enable 8uA current source.
0100 Enable 4uA current source.
0010 Enable 2uA current source.
0001 Enable 1uA current source.
PUD Pull up Resistor
1000 Enable 5K resistor source.
0100 Enable 10K resistor source.
0010 Enable 20K resistor source.
0001 Enable 40K resistor source.

91h Sleep Mode Raw Count Register 1 (RO)

Bit	D7:D0
Name	SLRC[15:8]
Default	0000 0000

92h Sleep Mode Raw Count Register 2 (RO)

Bit	D7:D0
Name	SLRC[7:0]
Default	0000 0000

SLRC Sleep Mode Raw Count
Read only. Value for reference

93h Sleep Mode Baseline Register 1 (RO)

Bit	D7:D0
Name	SLB[15:8]
Default	0000 0000

94h Sleep Mode Baseline Register 2 (RO)

Bit	D7:D0
Name	SLB[7:0]
Default	0000 0000

SLB Sleep Mode Baseline
Read only. Value for reference

95h Key Scan Once Register (RW)

Bit	D7:D2	D1	D0
Name	-	TR	EN
Default	000000	0	0

TR

Write 1 Trigger one scan
Read 1 Busy
Read 0 Data ready

EN Enable Key Scan Once
0 Continuous scan of all enabled keys
1 Scan all enabled keys once

96h Table Ready Mark Register (RO)

Bit	D7	D6:D0
Name	INIRDY	MARK[6:0]
Default	0	0000000

INIRDY Touch Key Init Ready
1 Touch key is initializing
0 Touch key initialization is completed

MARK This register is used by firmware to indicate parameters are correctly programmed.
Ready/Fail status
00 ready
Others not ready

7. BUZZER / MELODY APPLICATION

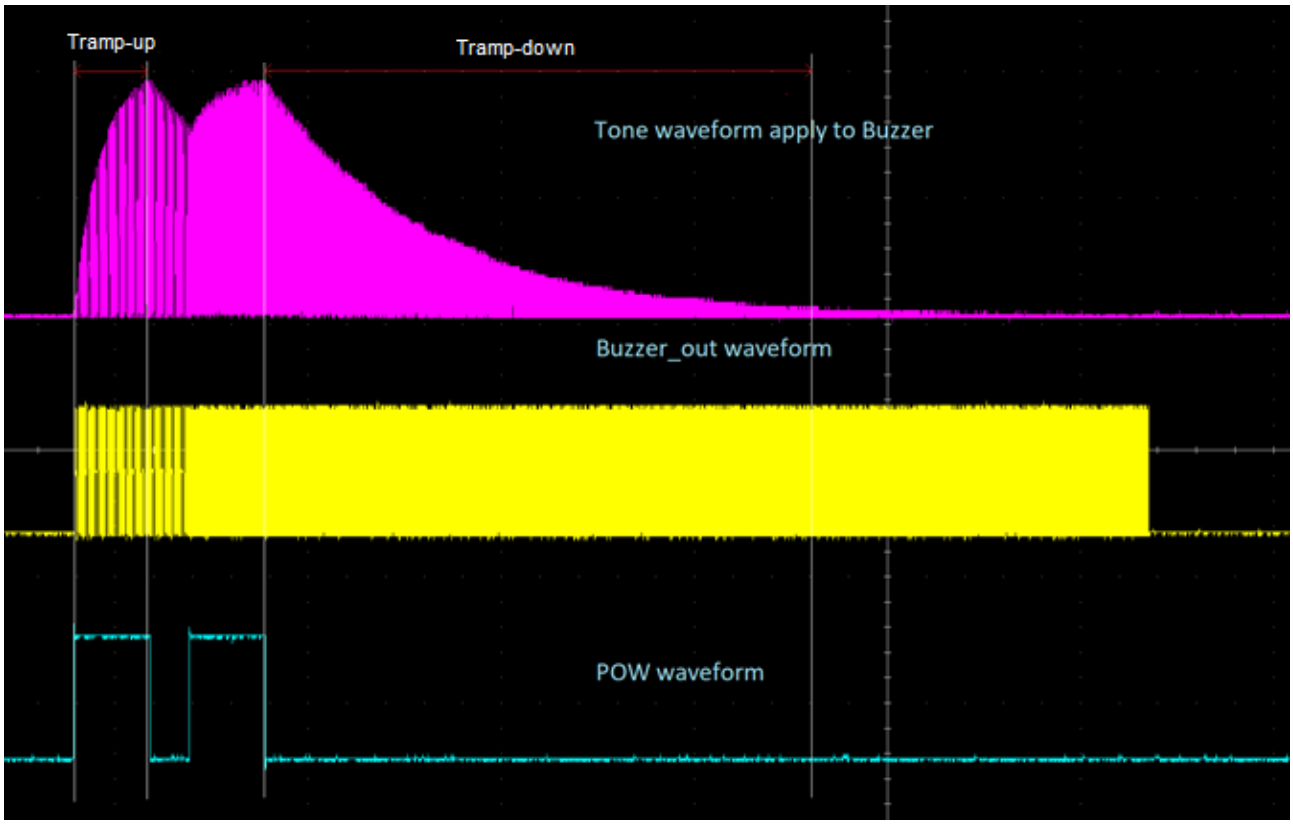


Figure 7-1 Buzzer/Melody Waveform

Note:

Tramp-up: 100R as below Figure 7-2decides the signal ramp-up rate.

Tramp-down: The signal ramps down because POW is low and 47uF capacitor as below Figure 7-2 decides the ramp- down rate.

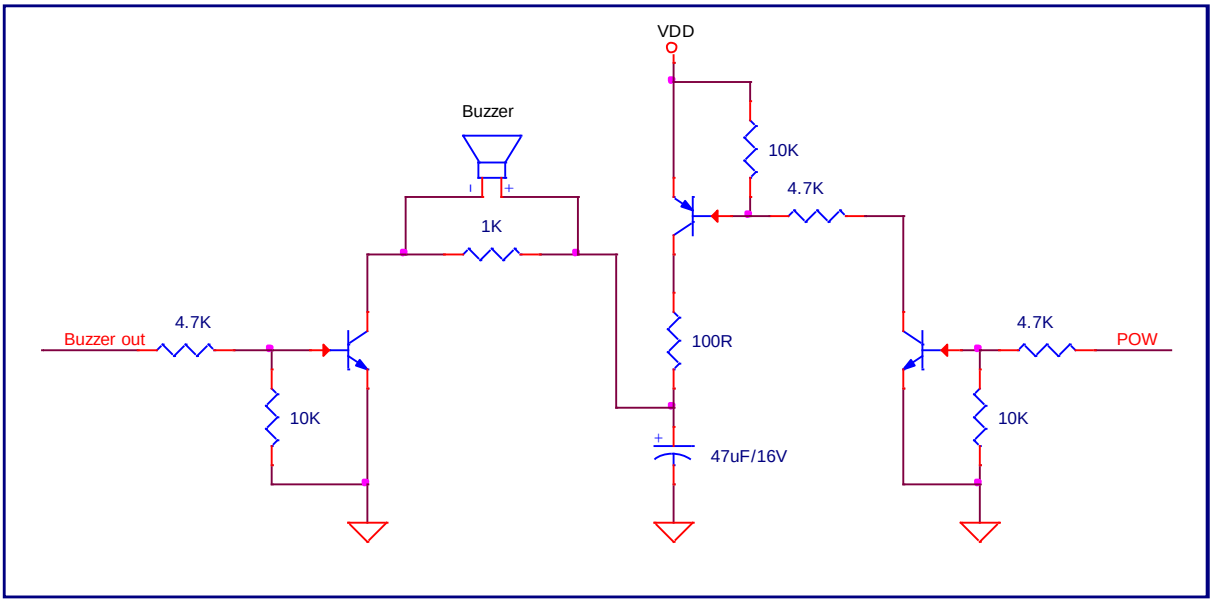


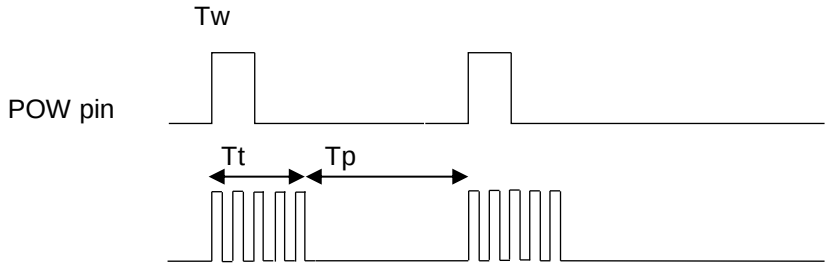
Figure 7-2 Typical Application Circuit for Melody

08h Buzzer Register (W)

Bit	D7:D0
Name	BW
Default	-

1st byte 2nd byte 3rd byte 4th byte

Scale ID	Tt	Tw	Tp



Buzzer out pin

Tt, Tw, and Tp range from 0 to 255 @ 4ms step

A Tone played duration is defined as Tt + Tp.

The support scale is from 3A to 8G#.

Frequencies for equal-tempered scale, A4 = 440 Hz
"Middle C" is C4

	3	freq	divisor	freq error	4	freq	divisor	freq error	5	freq	divisor	freq error
C					3	261.6	1911	0.01%	15	523.3	956	-0.05%
C#					4	277.2	1804	-0.01%	16	554.4	902	-0.01%
D					5	293.7	1703	-0.02%	17	587.3	851	0.04%
D#					6	311.1	1607	0.00%	18	622.3	804	-0.06%
E					7	329.6	1517	-0.01%	19	659.3	758	0.06%
F					8	349.2	1432	-0.02%	20	698.5	716	-0.02%
F#					9	370.0	1351	0.03%	21	740.0	676	-0.05%
G					10	392.0	1276	-0.04%	22	784.0	638	-0.04%
G#					11	415.3	1204	-0.01%	23	830.6	602	-0.01%
A	0	220.0	2273	-0.01%	12	440.0	1136	0.03%	24	880.0	568	0.03%
A#	1	233.1	2145	0.01%	13	466.2	1073	-0.04%	25	932.3	536	0.05%
B	2	246.9	2025	-0.01%	14	493.9	1012	0.04%	26	987.8	506	0.04%
	6	freq	divisor	Freq error	7	freq	divisor	Freq error	8	freq	divisor	Freq error
C	27	1046.5	478	-0.05%	39	2093.0	239	-0.05%	51	4186.0	119	0.37%
C#	28	1108.7	451	-0.01%	40	2217.5	225	0.21%	52	4434.9	113	-0.23%
D	29	1174.7	426	-0.08%	41	2349.3	213	-0.08%	53	4698.6	106	0.39%
D#	30	1244.5	402	-0.06%	42	2489.0	201	-0.06%	54	4978.0	100	0.44%
E	31	1318.5	379	0.06%	43	2637.0	190	-0.21%	55	5274.0	95	-0.21%
F	32	1396.9	358	-0.02%	44	2793.8	179	-0.02%	56	5587.7	89	0.54%
F#	33	1480.0	338	-0.05%	45	2960.0	169	-0.05%	57	5919.9	84	0.55%
G	34	1568.0	319	-0.04%	46	3136.0	159	0.28%	58	6271.9	80	-0.35%

Frequencies for equal-tempered scale, A4 = 440 Hz "Middle C" is C4												
G#	35	1661.2	301	-0.01%	47	3322.4	150	0.33%	59	6644.9	75	0.33%
A	36	1760.0	284	0.03%	48	3520.0	142	0.03%				
A#	37	1864.7	268	0.05%	49	3729.3	134	0.05%				
B	38	1975.5	253	0.04%	50	3951.1	127	-0.36%				

Scale ID(Sid): 0 is 3A, 1 is 3A#, 2 is 3B ….

08h Buzzer Register (W)

Bit	D7:D0
Name	BW
Default	0000 0000

Write melody data, stop melody play and clear the FIFO

08h Buzzer Register (R)

Bit	D7:D0
Name	BR
Default	0000 1010

BR Buzzer Register Read. It shows the available tone buffer size. SE5118A has 10 built-in note buffers.

I2C command format - Each node is composed of 4 byte data and the incomplete note will be ignored. The incoming note data will be ignored when the FIFO is full.

0x78, 0x07, (Sid, Tt, Tw, Tp), (Sid, Tt, Tw, Tp), ….

0x78, 0x07, 0xFF stops the melody play and clear the FIFO.

0x78, 0x07 Set the register number 0xF0.

0x79 Read FIFO’s remaining length.

8. TYPICAL APPLICATION INFORMATION

GENERAL DESCRIPTION

The IS32SE5118A is an ultra-low power, fully integrated 8-channel solution for capacitive touch-buttons applications. The chip allows electrodes to project sense fields through any dielectric material such as glass or plastic.

8.1 SENSITIVITY ADJUSTING

Sensitivity can be adjusted by the external capacitor or internal register. A higher capacitor value will yield out lower detect sensitivity. A lower capacitor value will yield out higher detect sensitivity.

8.2 INTERRUPT

Touch key detection event will trigger INT pin. The INT pin will be driven low when the selected channel is pressed.

9. CLASSIFICATION REFLOW PROFILE

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time between 25°C to peak temperature	8 minutes max.

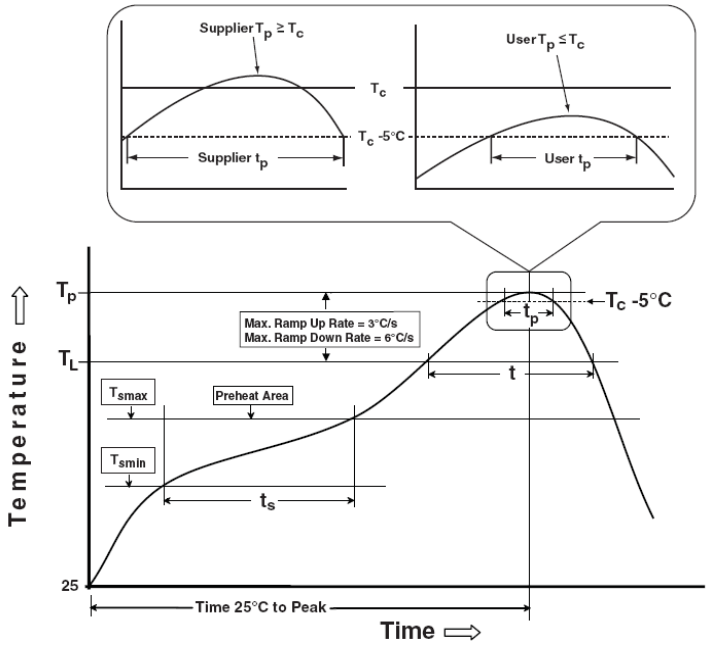
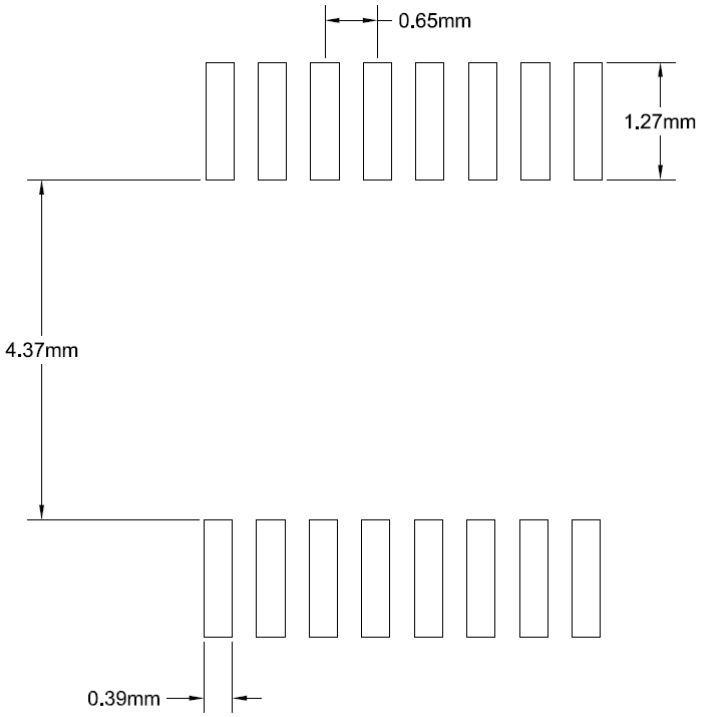


Figure 9-1 Classification Profile

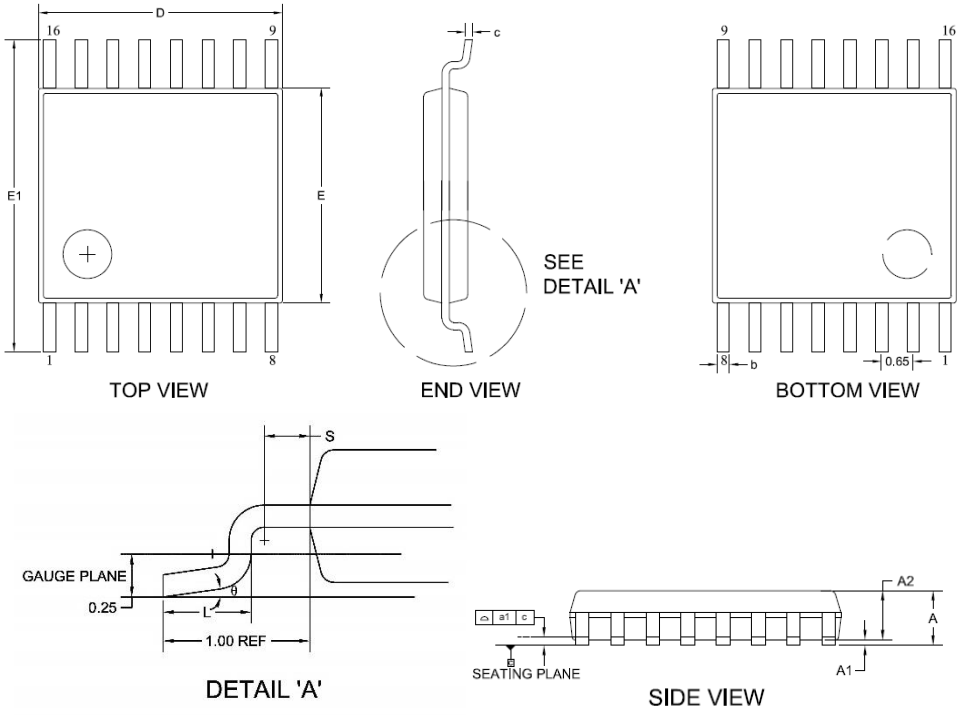
10. PACKAGE INFORMATION

10.1 TSSOP-16

10.1.1 RECOMMENDED LAND PATTERN



10.1.2POD



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
D	4.90	5.00	5.10
E	4.30	4.40	4.50
E1	6.40BSC		
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20		
c	0.09	—	0.20
θ	0°		8°
a1	0.10		

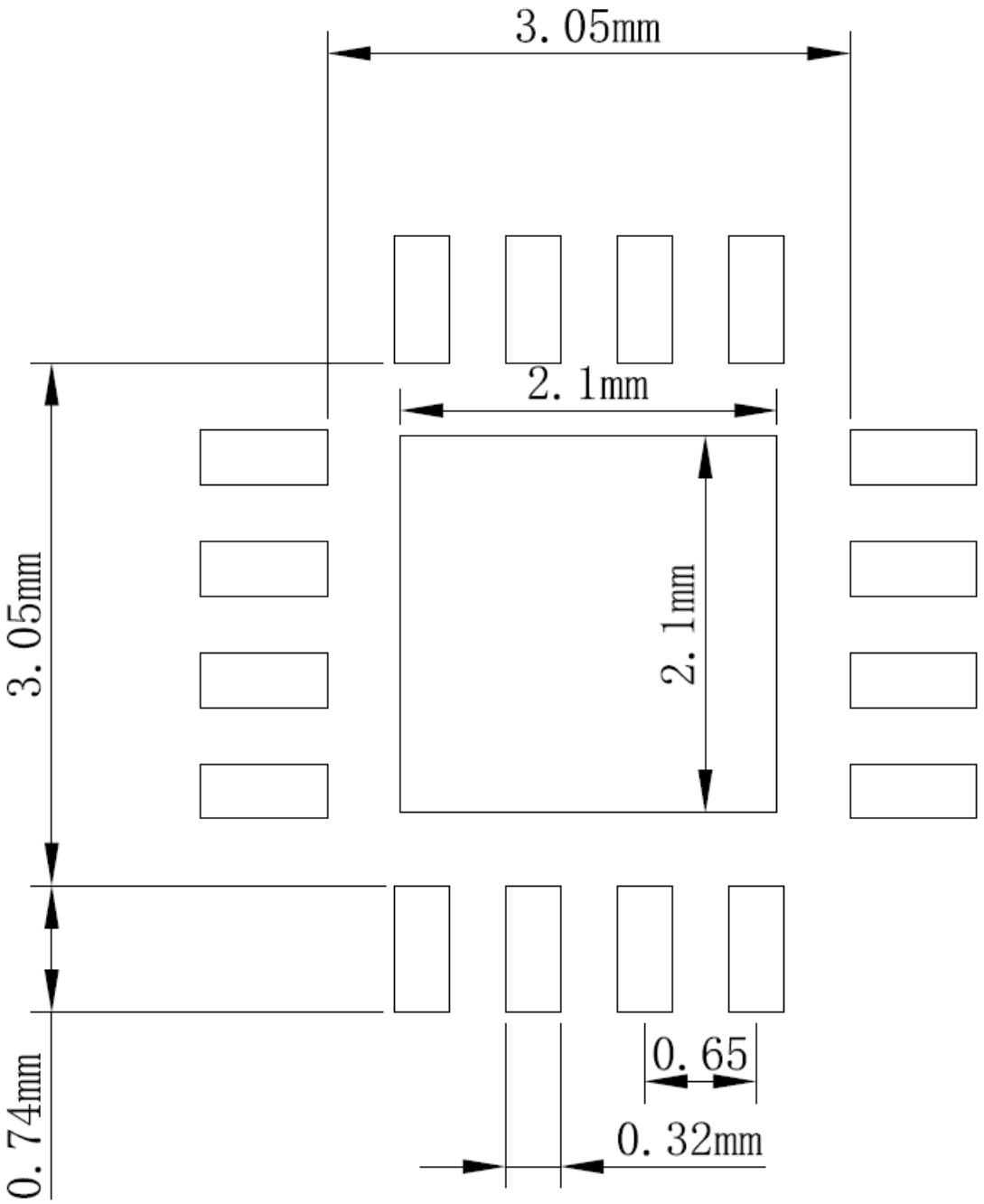
NOTES:

1. CONTROLLING DIMENSION: MM

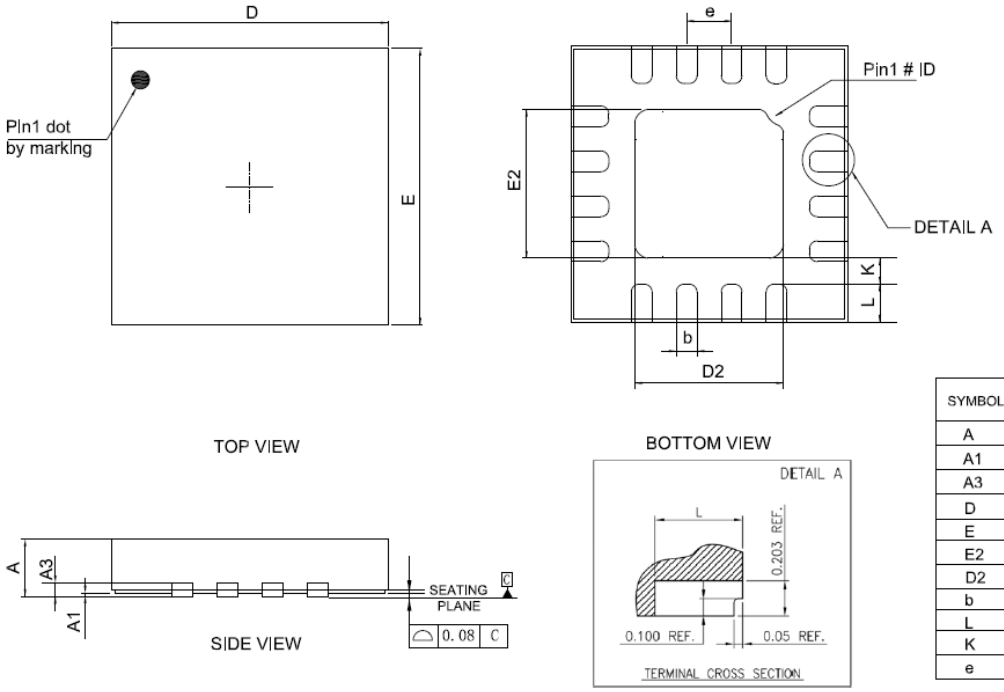
2. REFERENCE DOCUMENT: JEDEC MO-153

10.2 WQFN-16

10.2.1 RECOMMENDED LAND PATTERN



10.2.2POD



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.20REF		
D	3.90	4.00	4.10
E	3.90	4.00	4.10
E2	2.05	2.10	2.15
D2	2.05	2.10	2.15
b	0.25	0.30	0.35
L	0.35	0.40	0.45
K	0.20	—	—
e	0.65 BSC		

NOTE:

1. CONTROLLING DIMESION: MM
2. REFERENCE DOCUMENT: JEDEC MO-220
3. THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFENENT SHAPE AMONG DIFFERENT FACTORIES.

11. REVISIONS

Revision	Detailed Information	Date
A	First Formal Release	2023.11.29