Features

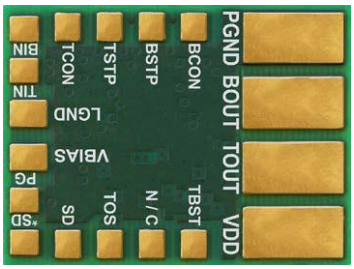
- 50 V_{DC}/10 A Fully De-Rated Device
- **Integrated Output eGaN® Power HEMTs**
- Four Possible Configurations:
  - Single Low-Side Gate Driver
  - Single High-Side Gate Driver
  - Independent Low- and High-Side Gate Drivers
  - Half-Bridge Gate Drivers with Input Shoot-through Protection
- Internal Shoot-Through Protection
- Internal Power Good Circuitry
- High Speed Switching Capability: 1.0+ MHz
- Rugged Compact Molded SMT Package
- "Pillar" I/O Pads
- eGaN® HEMT Switching Elements
- Commerce Rated EAR-99

Development Vehicle for:

- **FBS-GAM02-P-C50 (Available) Commerce Rated 9A515.X**

Application

- Development Vehicle for FBS-GAM02-P-C50
- Power Switches/Actuators
- Single and Multi-Phase Motor Phase Drivers
- Point-Of-Load Building Block
- High Speed DC-DC Conversion



FBS-GAM02-P-C50

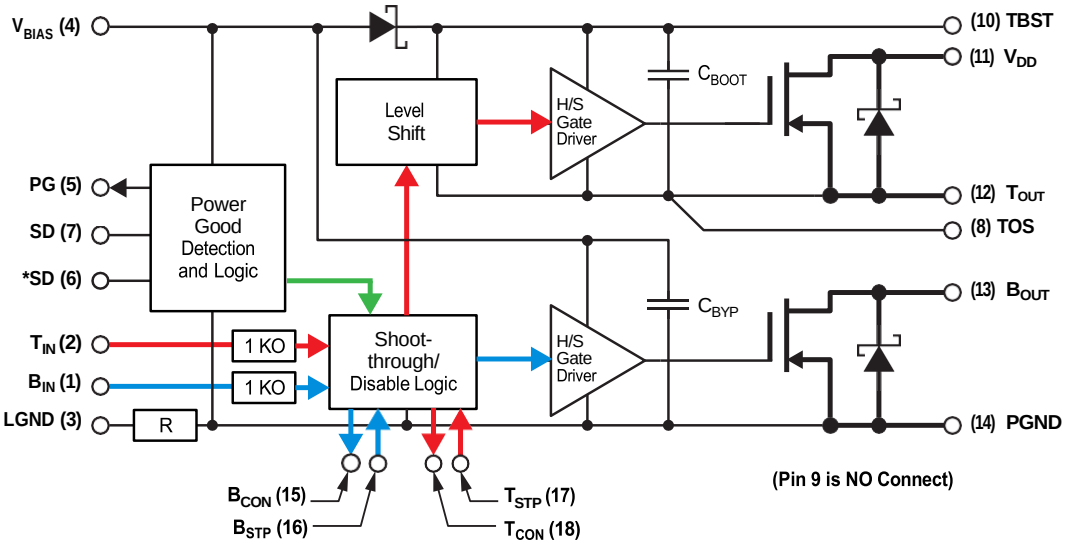
50 V_{DC} / 10 A Multifunction Power Module Development Vehicle

Description

EPC Space's **FBS-GAM02-P-C50** Multi-Function Power Module incorporate eGaN® switching power HEMTs-offered as the **non-flight development vehicle** to EPC Space's **FBS-GAM02-P-R50** commercial space device, or a standalone full featured industrial device. These modules include two *100 Volt Rated Output Power Switches,* two high speed *gate drive circuits* (**consisting entirely of eGaN® switching elements**), two power Schottky diode clamp elements with *shoot-through prevention logic* (for the Half-Bridge connection) and a +5 V_{DC} gate drive bias "power good" monitoring circuitry in an innovative, space-efficient, 18 pin SMT molded epoxy package under US Patent #10,122,274 B2.

Commerce Rated EAR-99 Device

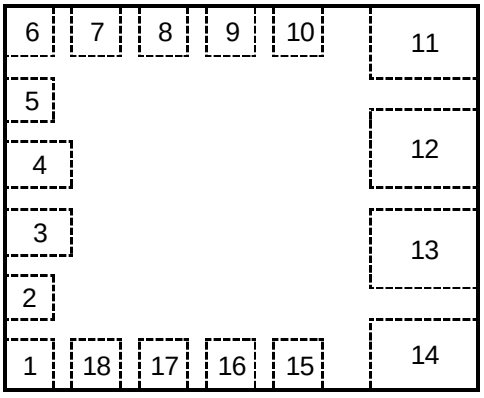
FBS-GAM02-P-C50 Functional Block Diagram



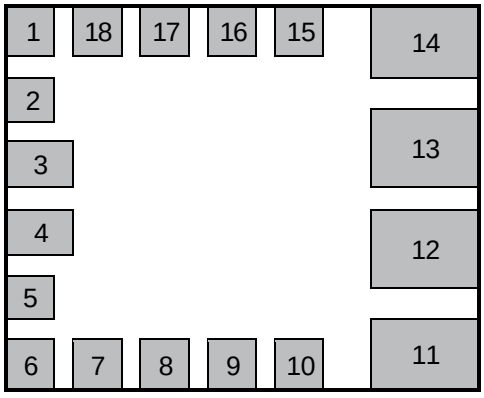
FBS-GAM02-P-C50 Functional Block Diagram

18 Pin Molded SMT Package with Pillar Pins

Top (X-Ray) View



Bottom (Pad) View



FBS-GAM02-P-C50 Configuration and Pin Assignment Table

Pin #	Pin Name	Input/Output	Pin Function
1	B_{IN}	I	Low-Side Switch Logic Input
2	T_{IN}	I	High-Side Switch Logic Input
3	LGND	--	Logic Ground, 0 V_{DC} (Low Current)
4	V_{BIAS}	I	+5 V_{DC} Gate Driver Power Supply Bias Input Voltage
5	PG	O	Power Good Logic Output (Open Drain)
6	*SD	I	Low True Shutdown Input
7	SD	I	High True Shutdown Input
8	TOS	I	High-Side Output (Switching Node) Sense
9	N/C	--	No Internal Connection
10	TBST	I	High-Side Bootstrap Potential
11	V_{DD}	I	Positive Power Input Supply Voltage (High Current)
12	T_{OUT}	O	High-Side Output, High Side Switch (High Current)
13	B_{OUT}	O	Low-Side Output, Low Side Switch (High Current)
14	PGND	--	Power Supply Return, 0 V_{DC} (High Current)
15	B_{CON}	I	Low-Side Switch Shoot Through Control Input
16	B_{STP}	O	Low-Side Switch Shoot Through Protection Output
17	T_{STP}	O	High-Side Switch Shoot Through Protection Output
18	T_{CON}	I	High-Side Switch Shoot Through Control Input

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Absolute Maximum Rating *(-40°C≤ TC ≤ 85°C unless otherwise)*

Symbol	Parameter-Conditions	Value	Units
V_{DS}	High Side Gate Driver Reference Voltage (Note 1)	50% Voltage De-Rating	V
		No Voltage De-Rating	
V(BEMF)	Half-Bridge-Connected BEMF Voltage at B_{OUT}/T_{OUT} Terminals: Motor Driver Coast Mode, Three Phase Voltage/Phase-to-Phase (Note 20)		V
I_D	Continuous Drain Current	10	A
V_{BIAS}	Continuous Gate Driver Bias Supply Voltage	-0.3 to 6.5	V
B_{IN}, T_{IN}	B_{IN} or T_{IN} Input Voltage	-0.3 to 5.0	
T_{STG}	Storage Junction Temperature Range	-55 to +140	°C
T_J	Operating Junction Temperature Range	-40 to +130	
T_c	Case Operating Temperature Range	-40 to +85	
T_{sol}	Package Mounting Surface Temperature	225	
ESD	ESD class level (HBM)	1A	

Thermal Characteristics

Symbol	Parameter-Conditions	Value	Units
$R_{\theta CA}$	Thermal Resistance Junction to Case, Either eGaN® Power Switch (Note 3)	8.5	°C/W
$R_{\theta JC}$	Thermal Resistance Junction to Case, Either Clamp Schottky Diode (Note 3)	20	

Low- and High-Side Power Switch Static Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Parameter	Symbol	Test Conditions		MIN	TYP	MAX	Units
Drain - Source Leakage Current	I_{DSS}	V_{DS} = 25 V_{DC}, B_{IN} = T_{IN} = 0.8 V_{DC}, (Note 1)	T_C = 25°C	-	10	125	µA
			T_C = 85°C	-	125	450	
		V_{DS} = 50 V_{DC}, B_{IN} = T_{IN} = 0.8 V_{DC}, (Note 1)	T_C = 25°C	-	25	170	
			T_C = 85°C	-	170	705	
		V_{DS} = 100 V_{DC}, B_{IN} = T_{IN} = 0.8 V_{DC}, (Note 1)	T_C = 25°C	-	95		
			T_C = 85°C	-	550		
Half-Bridge-Connected Back-EMF (BEMF) Leakage Current: Motor Driver Coast-Mode	I_{BEMF}	BEMF = 15 V_{pk}, B_{IN} = T_{IN} = 0.8 V_{DC}, (Notes 10, 12, 20)	T_C = 25°C		60		mA_{pk}
Drain - Source ON-State Resistance	$R_{DS(on)}$	I_D = 10 A (Note 2)	T_C = 25°C		10	18.5	mΩ
			T_C = 85°C	-	12	28	
			T_C = -40°C		9	15	
Drain - Source ON-State Resistance	V_{SD}	I_D = 10 A (Note 2)	T_C = 25°C		0.90	0.97	V
			T_C = 85°C		0.83	0.90	
			T_C = -40°C		0.97	1.15	

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B_{IN}, T_{IN} Logic Input Static Electrical Characteristics *(-40°C≤ TC ≤ +85°C unless otherwise noted)*

Parameter	Symbol	Test Conditions		MIN	TYP	MAX	Units
Low Logic Level Input Voltage	V_{IL}	V_{BIAS} = 5 V_{DC} (Note 5)				0.8	V
High Logic Level Input Voltage	V_{IH}	V_{BIAS} = 5 V_{DC} (Note 6)		2.9			
Low Logic Level Input Current	I_{IL}	V_{BIAS} = 5 V_{DC}, V_{IL} = 0.4 V	T_C = 25°C	-5	+/-1	5	µA
			T_C = 85°C	-50	+/-10	50	
High Logic Level Input Current	I_{IH}	V_{BIAS} = 5 V_{DC}, V_{IL} = 3 V	T_C = 25°C	-5	+/-1	5	µA
			T_C = 85°C	-50	+/-10	50	
High Logic Level Shoot-Through-State Logic Input Current	I_{IHST}	V_{BIAS} < UVLO- or V_{BIAS} > OVLO+ B_{IN} = T_{IN} = 3.0 V_{DC}	T_C = 25°C		3		mA

VDD-to-PGND Static Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
SN-to-PGND Operating Voltage Range	VDD-to-PGND	(Note 3)	5		50	V

V_{BIAS} Static Electrical Characteristics *(-40 < T_C <85°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
V_{BIAS} Recommended Operating Voltage Range	V_{BIAS}	V_{BIAS} = 5 V_{DC} (Note 9)	4.75	5.05	5.25	V
V_{BIAS} Operating Current	I_{BIAS}	V_{BIAS} = 5.5 V_{DC}		16	20	mA

PG Logic Output Static Electrical Characteristics *(-40 < T_C <85°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Low Logic Level Output Voltage	V_{OL}	V_{BIAS} ≥ 2.3 V_{DC} (Notes 6, 7, 22)			0.2	V
High Logic Level Output Voltage	V_{OH}	V_{BIAS} > UVLO+ (Notes 6, 7)	3.5			
Low Logic Level Output Current	I_{OL}	V_{BIAS} < UVLO- (Note 8, 22)			5	mA
High Logic Level Output Leakage Current	I_{OH}	V_{BIAS} = 5.25 V_{DC} (Note 8)		100		µA

PG Functional Static Electrical Characteristics *(-40 < T_C <85°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
V_{BIAS} UVLO Rising Threshold	UVLO+	(Notes 6, 7, 8, 9)			4.7	V
V_{BIAS} UVLO Falling Threshold	UVLO-		2.95			
UVLO Hysteresis	UVLO+ - UVLO-			0.2		
V_{BIAS} OVLO Indicator Rising Threshold	OVLO+			6.70		
V_{BIAS} OVLO Indicator Falling Threshold	OVLO-		5.55			
OVLO Hysteresis	OVLO+ - OVLO-			0.12		

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Independent Low- and High-Side Power Switch Dynamic Electrical Characteristics

(T_C = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
B_{IN}-to-B_{OUT} Turn-ON Delay Time	$t_{d(on)}$	V_{DS} = 25 V_{DC}; I_D = 3 A (See Switching Figures)		45	110	ns
B_{OUT} Rise Time	t_r			10.5	28	
B_{IN}-to-B_{OUT} Turn-OFF Delay Time	$t_{d(off)}$			45	100	
B_{OUT} Fall Time	t_f			5	25	
T_{IN}-to-T_{OUT} Turn-ON Delay Time	$t_{d(on)}$	V_{DS} = 25 V_{DC}; I_D = 3 A (See Switching Figures)		60	150	
T_{OUT} Rise Time	t_r			6.5	25	
T_{IN}-to-T_{OUT} Turn-OFF Delay Time	$t_{d(off)}$			75	190	
T_{OUT} Fall Time	t_f			6	25	

User Half-Bridge Configuration Dynamic Electrical Characteristics

(T_C = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Half-Bridge Configuration B_{OUT}-to-T_{OUT} and T_{OUT}-to-B_{OUT} Dead Time	t_{dt}	(Notes 3, 12, 15)	60			ns
B_{IN} Falling-to-T_{IN} Rising Delay Time	t_{d1}	(Notes 3, 12, 21)	70			
T_{IN} Falling-to-B_{IN} Rising Delay Time	t_{d2}	(Notes 3, 12, 21)	122			

Half-Bridge Configuration Schottky Catch Diode Transient Electrical Characteristics

(T_C = 85°C unless otherwise noted)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Peak Pulse Forward Current	$I_{F(pk)}$	B_{IN} = T_{IN} = 0.8 V_{DC}; 13 V_{DC} < V_{DD} < 22 V_{DC} (Notes 3, 18)			9.1	A

Half-Bridge Configuration Low- and High-Side Power Switch Transient Electrical Characteristics

(T_C = 85°C unless otherwise noted)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Peak Pulse Drain Current	$I_{D(pk)}$	f_s = 400 kHz; 10% < Duty Cycle < 90%; 30 ns < Dead Time < 50 ns; 13 V_{DC} < V_{DD} < 50 V_{DC}, V_{BIAS} = 5 V_{DC} (Notes 3, 19)			15	A

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Module Dynamic Electrical Characteristics *(T_C = 25°C unless otherwise noted)*

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
Power Switch Output Capacitance	C_{OSS}	B_{OUT}-PGND or V_{DD}-T_{OUT} = 5 V_{DC}		1150		pF
		B_{OUT}-PGND or V_{DD}-T_{OUT} = 50 V_{DC}		500		
Dynamic Gate/Driver Losses	P_{GD}	V_{BIAS} = 5 V_{DC}		21		mW/MHz
Internal Bootstrap Capacitance	C_{boot}			47		nF
External Bootstrap Capacitance	C_{boot} (ext)				1	µF
LGND-PGND Resistance	R_G			1		Ω
High Side Power Switch Start Up Pre-Charge Time: Half Bridge Configuration	t_{prg}	(Notes 3, 10, 11, 12)	5			µs
High Side Power Switch Maximum Duty Cycle	$t_{d/c}$				95	%
Minimum Switching Frequency: Low-side Power Switch	f_s	(Notes 3, 10, 11, 12, 13, 14, 15, 16)	0			Hz
Minimum Switching Frequency: High-side Power Switch			200			kHz
Maximum Switching Frequency: Half-Bridge Configuration				1	TBD	MHz
Shoot-Through Protection Activation Delay Time	t_{st}	(Notes 3, 14)		5		ns

Specification Notes

1.) V_{BIAS} = 5 V_{DC}, PGND = LGND = 0 V_{DC}, V_{DS} = V_{DD}-to-T_{OUT} = 50 V_{DC} or V_{DS} = B_{OUT}-to-PGND as specified.

2.) Measured using 4-Wire (Kelvin) sensing techniques.

3.) Guaranteed by design. Not tested in production.

4.) When either logic input (B_{IN} or T_{IN}) is at the low input voltage level the associated output (B_{OUT} or T_{OUT}) is guaranteed to be OFF (high impedance).

5.) When either logic input (B_{IN} or T_{IN}) is at the low input voltage level the associated gate drive output (B_{OUT} or T_{OUT}) is guaranteed to be ON (low impedance).

6.) Parameter measured with a 4.7kΩ pull-up resistor between PG and V_{BIAS}.

7.) PG is at a low level when V_{BIAS} is below the UVLO- (falling) threshold level or the OVLO+ (rising) threshold level. PG is at a high level when V_{BIAS} is above the UVLO+ (rising) threshold level or the OVLO- (falling) threshold level.

8.) PG is an open drain output referenced to LGND.

9.) V_{BIAS} levels below the UVLO- and above the OVLO+ thresholds result in the low-side and high-side gate drivers being disabled: The logic inputs to the drivers are internally set to a logic low state (i.e. OFF) to prevent damage to the external EPC Space eGaN® HEMT power switches.

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Specification Notes *(continued)*

10.) The high side gate driver utilizes a bootstrap capacitor to provide the proper bias for this circuit. As such, this capacitor **MUST** be periodically re-charged from the V_{BIAS} supply. As a stand-alone high-side switch with a ground-connected/ground-sensed load, this recharging takes place each time the switch is turned OFF and the TOUT node returns to ground potential (0 V_{DC}). However, when connected in conjunction with the low-side power switch in the half-bridge configuration, this connection to ground does not exist until the low-side power switch is turned ON, thus creating a low impedance connection from T_{OUT} through the low-side power switch (B_{OUT}-PGND). The time t_{prg} is the minimum time required to ensure that the bootstrap capacitor is properly charged when power is initially applied to the FBS-GAM02-P-C50 Module.11.) The minimum frequency of operation is determined by the internal bootstrap capacitance and the bias current required by the high side gate driver circuit.

11.) The minimum frequency of operation is determined by the internal bootstrap capacitance and the bias current required by the high-side power switch gate driver circuit. In order to keep the high-side power switch gate driver bootstrap capacitor properly charged it is recommended that the maximum duty cycle ($t_{on} \cdot f_s$) of the high-side power switch is limited to the value shown. Accordingly, the high-side power switch is unsuitable for DC applications with the use of an external DC power supply connected between the TBST(+) and TOS(-) pins.

12.) For half-bridge applications, a “dead” time delay MUST be added between the time when the B_{OUT} output transitions ON-TO-OFF and the T_{OUT} output transitions OFF-to-ON, and also when the T_{OUT} output transitions ON-to-OFF and the B_{OUT} output transitions OFF-to-ON, to avoid both power switches being actuated simultaneously. Simultaneous actuation of the high-side and low-side power switches causes very large, uncontrolled and destructive currents to flow through the ON-state switches from V_{DD} to PGND. In order to calculate the desired output dead times (t_{DEAD}), the delay time from B_{IN} transitioning from logic 1-to-0 to T_{IN} transitioning from logic 0-to-1 is:

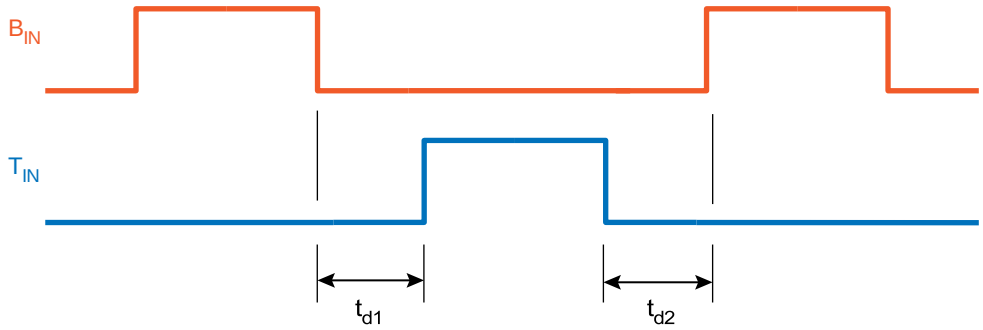
$$t_{d1} = (t_{LSd(OFF)} + t_{LSf}) + t_{DEAD} - (t_{HSd(ON)} + t_{HSr}),$$

where the LS nomenclature refers to the low-side driver off-delay and fall times and the HS nomenclature refers to the high-side driver on-delay time and rise time.

The delay time from T_{IN} transitioning from logic 1-to-0 to B_{IN} transitioning from logic 0-to-1 is:

$$t_{d2} = (t_{HSd(OFF)} + t_{HSf}) + t_{DEAD} - (t_{LSd(ON)} + t_{LSr}),$$

where the HS nomenclature refers to the high-side driver off-delay and fall times and the LS nomenclature refers to the low-side driver on-delay time and rise time.



13.) The maximum dead time prevents the Schottky clamp diodes in the power switch outputs from being overstressed and damaged by excessive power dissipation. The maximum dead time is limited by the switching frequency and by the power dissipation of the Schottky diodes: $P_d = V_f \cdot I_o \cdot 2 \cdot t_d/T$. Please refer to Figures 28, 29, and 31.

14.) The input shoot-through protection is activated if both the B_{IN} and T_{IN} logic inputs are set to the logic high (“1”) condition simultaneously. In the case where the B_{IN} and T_{IN} inputs are set to logic high, both the low- and high-side power switches are set to their high impedance (OFF) state.

15.) V_{DD} = 50 V_{DC}, I_D = +/-10 A and f_s = 1.0 MHz. Half-bridge configuration.

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Specification Notes *(continued)*

16.) The maximum switching frequency is limited by power dissipation in the half-bridge configuration, and not by throughput delay times. Faster switching frequencies are possible at reduced V_{DD} and Io operating levels and at reduced ambient operating temperatures. See Figures 24 through 27.

17.) See Figure 23.

18.) Half-bridge configuration. Current from pin 12 to pin 11 (high-side Schottky) or pin 14 to pin 13 (low-side Schottky), not drawn simultaneously. Pulse duration = 500 µs. Repetition rate = 5 seconds.

19.) Half-bridge configuration. Current from pin 11 to pin 12 or pin 12 to pin 11 (High-side Power Switch), or pin 13 to pin 14 or pin 14 to pin 13 (low-side Power Switch), not drawn simultaneously. Pulse duration = 500 µs. Repetition rate = 5 seconds.

20.) When connected in the half-bridge configuration and with a motor load in the coast mode (B_{IN} = T_{IN} = low logic level), the motor back-EMF (B_{EMF}) caused by rotation (generator effect) will cause a “leakage” current to flow into the switching node of the GAM02 module (B_{OUT}/T_{OUT} common connection). This leakage current is due to the high-side driver biasing circuitry. Due to the power ratings of the internal components, the peak value of the BEMF should be limited to that value shown in the Absolute Maximum Ratings. Additionally, when operating in the coast mode, in order to guarantee proper operation of the half-bridge circuit, the high-side driver bootstrap capacitor **MUST** be recharged periodically in order to assure that the high-side gate driver is biased properly, and that the high-side power switch responds correctly to the T_{IN} logic input. If the high-side bootstrap capacitor is not periodically recharged, then potentially destructive currents may flow in the GAM02 module.

21.) Setting the B_{IN}-to-T_{IN} and T_{IN}-to-B_{IN} delay times, t_{d1} and t_{d2}, to the values shown in the table guarantees shoot-through free operation of the GAM02 module when connected in the half-bridge configuration.

22.) Refer to Figure 6 for PG characteristic when VBIAS < 2.3V.

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Switching Figures

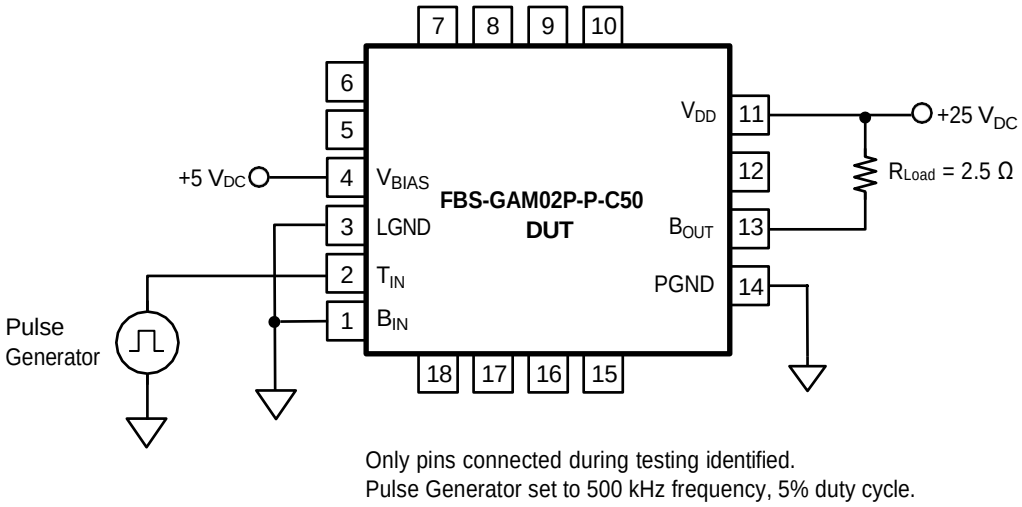
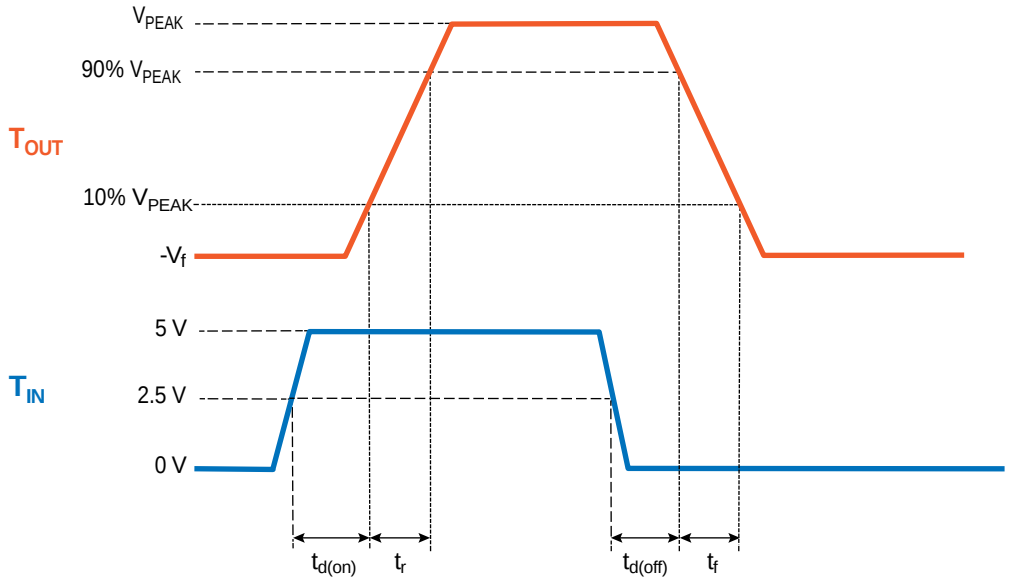


Figure 1. T_{IN}-to-T_{GATE} Switching Time Test Circuit



NOTE: Waveforms exaggerated for clarity and observability.

Figure 2. T_{IN}-to-T_{OUT} Switching Time Definition

Switching Figures *(continued)*

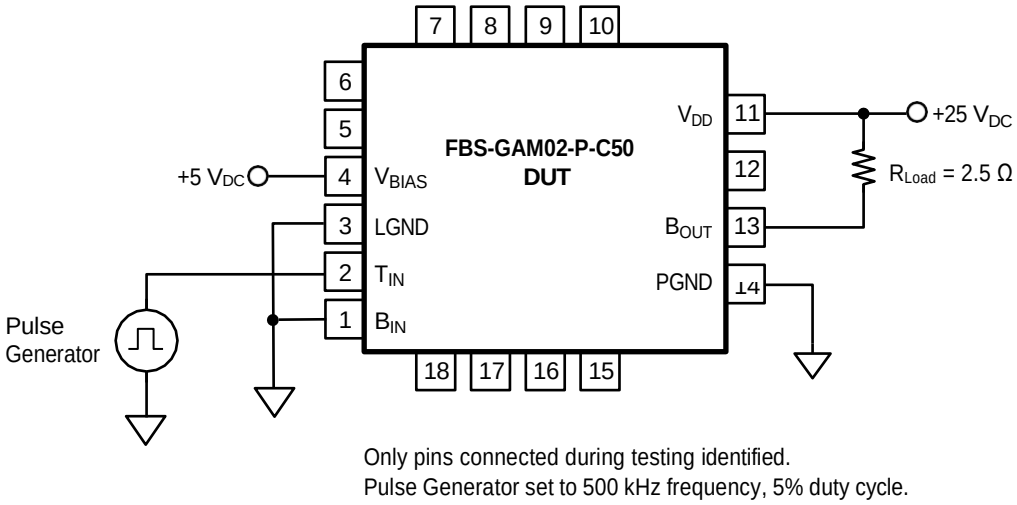
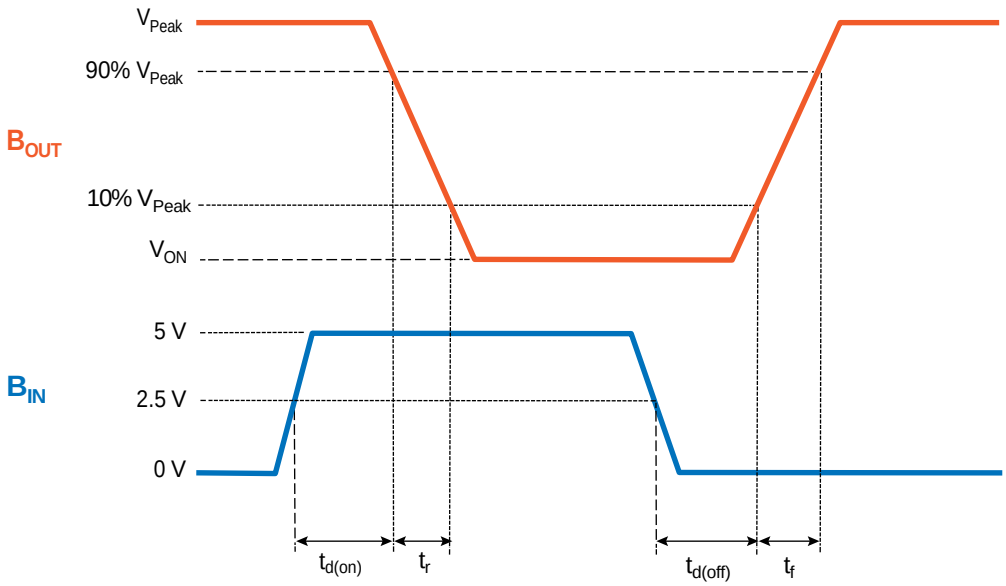


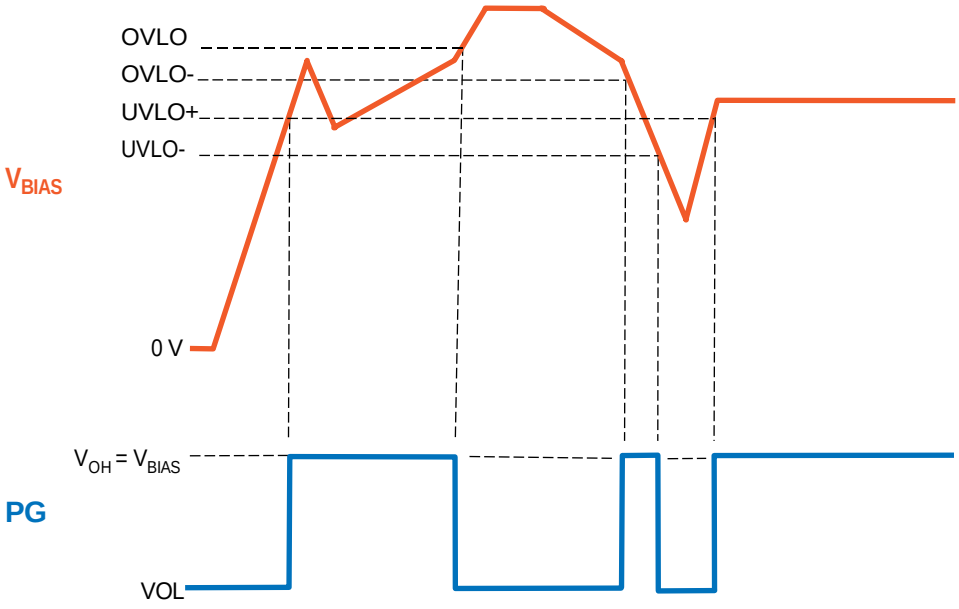
Figure 3. B_{IN}-to-B_{OUT} Switching Time Test Circuit



NOTE: Waveforms exaggerated for clarity and observability.

Figure 4. B_{IN}-to-B_{OUT} Switching Time Definition

Switching Figures *(continued)*



NOTE: Waveforms exaggerated for clarity and observability.

Figure 5. V_{BIAS}-to-PG Relationship

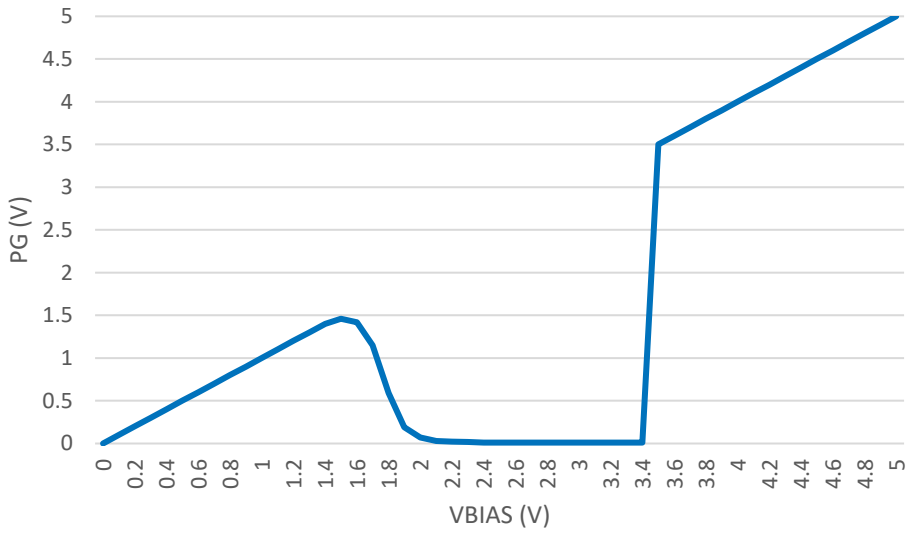


Figure 6. Typical PG Output vs V_{BIAS} Input

Typical Application Information

The following figures detail the suggested applications for the FBS-GAM02-P-C50 Module. For all applications, please refer to the Implementation section, following, for proper power supply bypassing and layout recommendations and criteria. In any of the following applications, if an inductive load is driven then an appropriately-rated Schottky rectifier/diode should be connected across the load to prevent destructive flyback/"kickback" voltages from destroying the FBS-GAM02-P-C50.

In all the following figures only the pins that are considered or that require connection are identified.

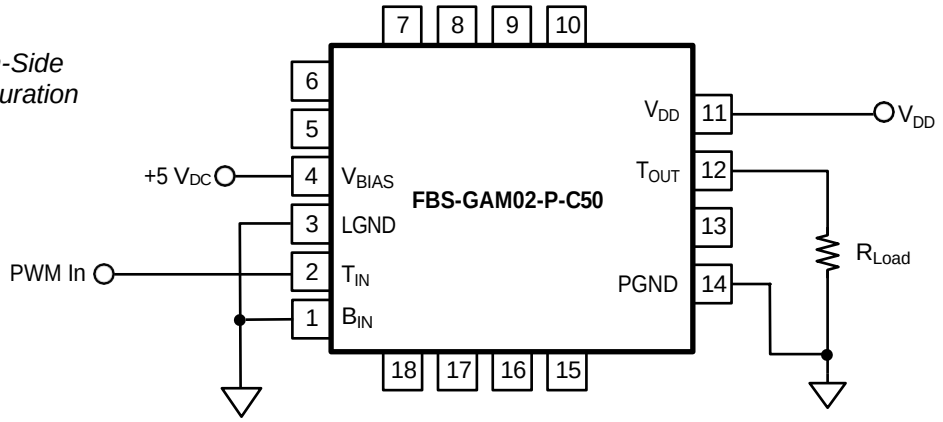


Figure 7. Single High-Side Power Switch Configuration

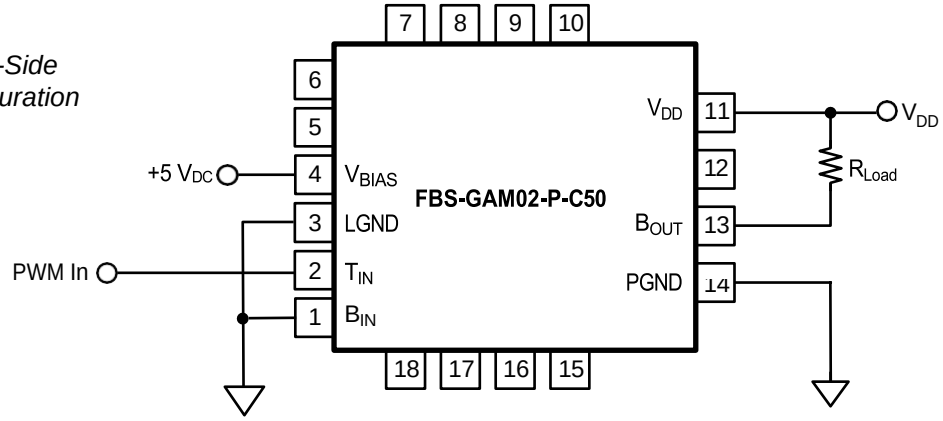


Figure 8. Single Low-Side Power Switch Configuration

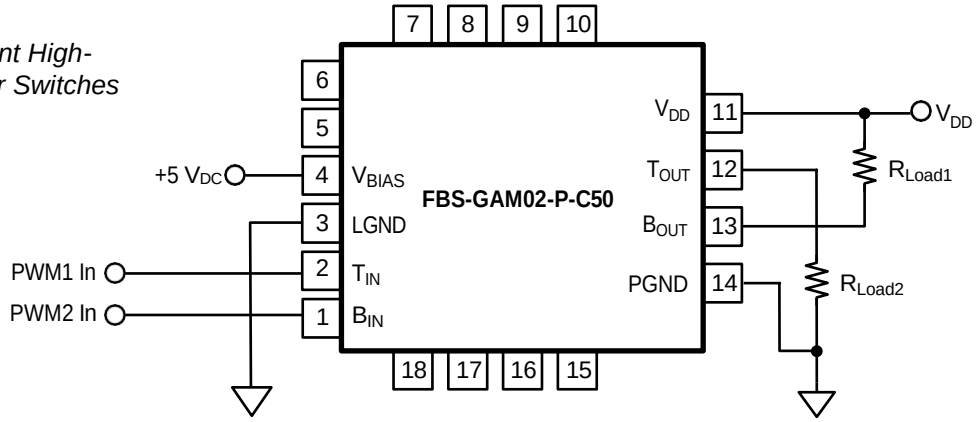


Figure 9. Independent High- and Low-Side Power Switches

Figure 10. Independent Switch Configuration: Two-Transistor Forward Converter Output Stage

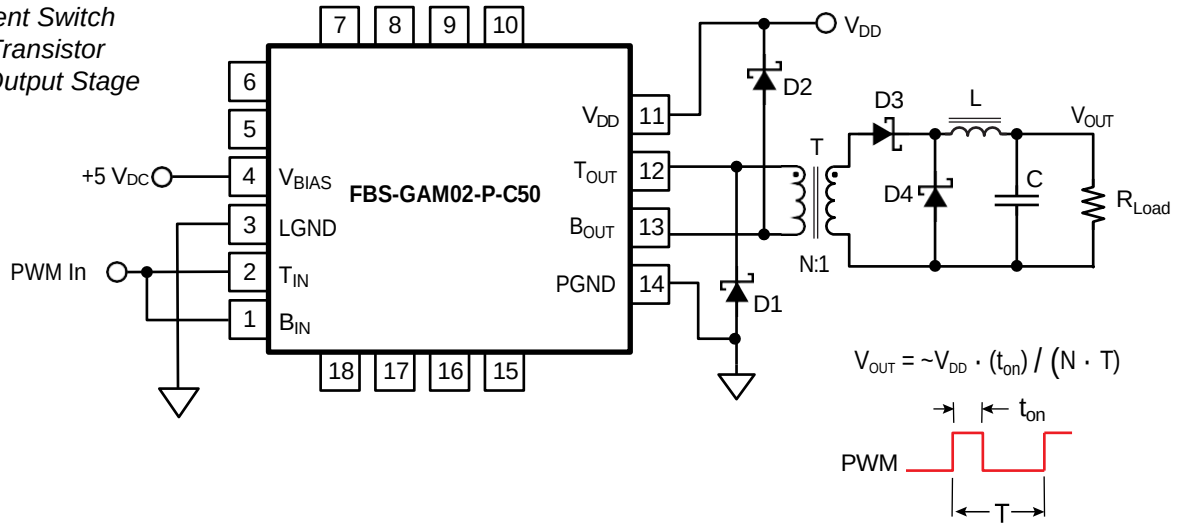
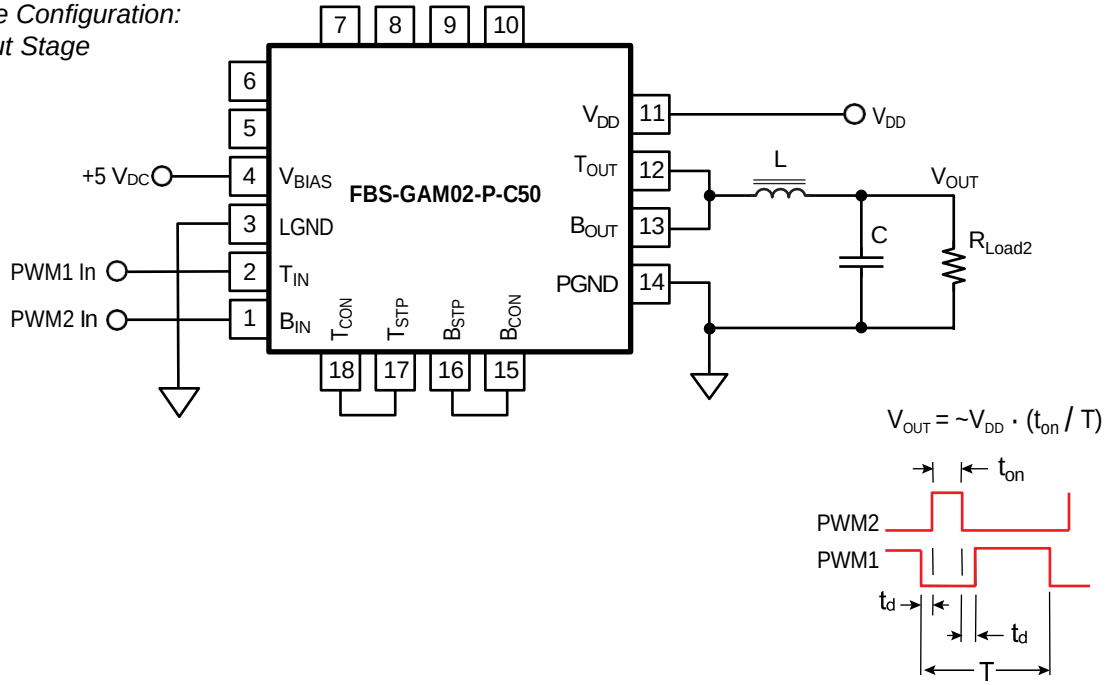


Figure 11. Half-Bridge Configuration: POL Converter Output Stage



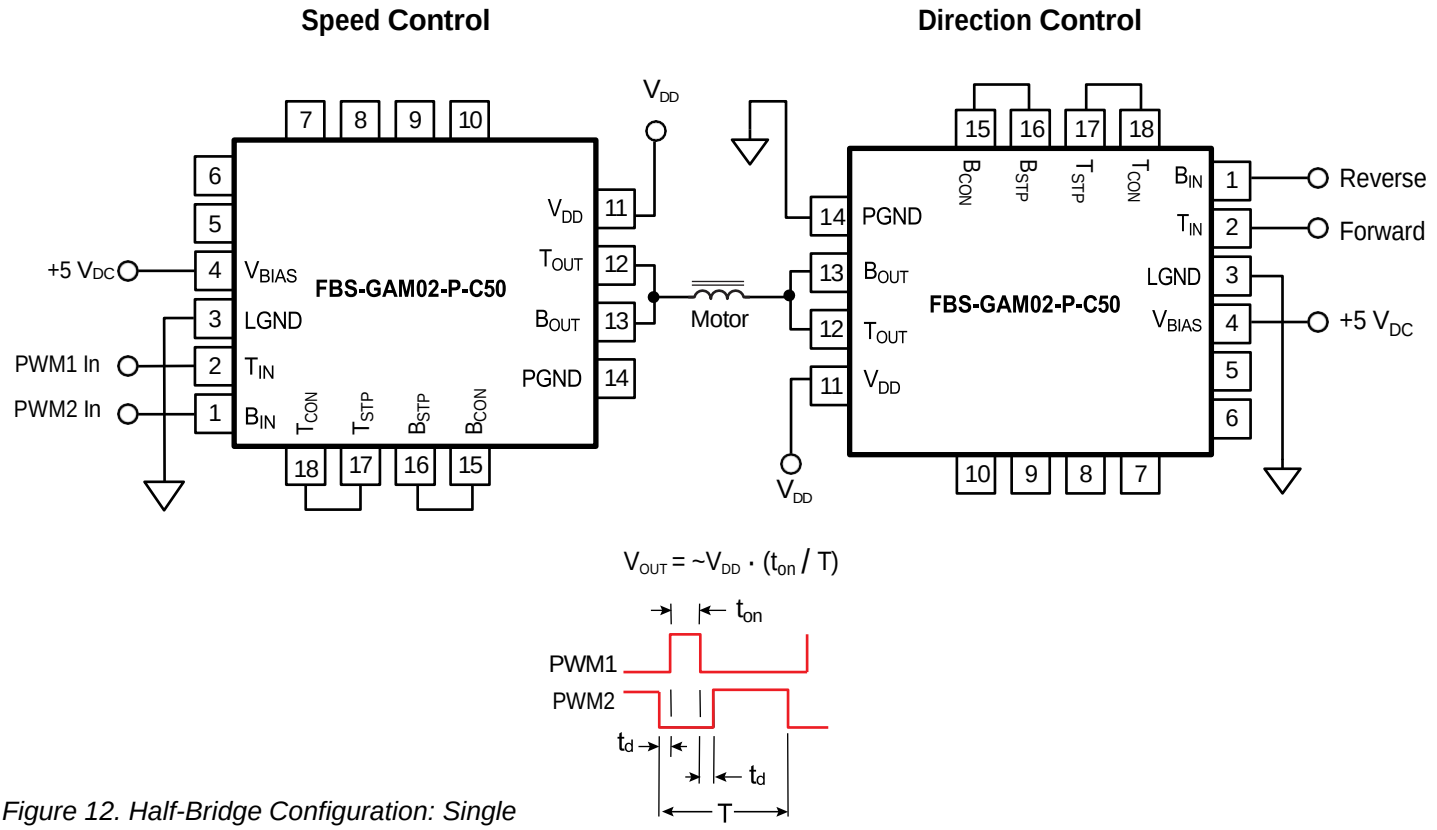


Figure 12. Half-Bridge Configuration: Single Phase Motor Drive Stage

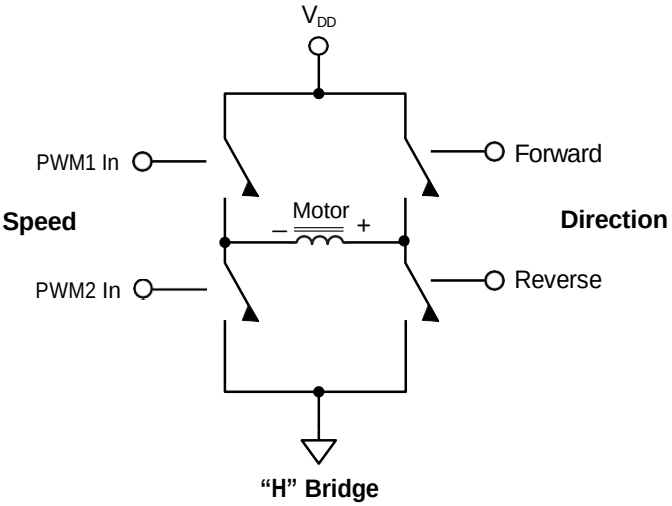


Figure 13. Half-Bridge Configuration: Single Phase Motor Driver Equivalent Circuit

Motor State Truth Table

PWM1	PWM2	Forward	Reverse	Motor Result (Direction/ Speed)
X	X	0	0	OFF/Coast Mode
Min D	Max D	1	0	Forward/Max Speed
Max D	Min D	1	0	Forward/Min Speed
Min D	Max D	0	1	Reverse/Min Speed
Max D	Min D	0	1	Reverse/Max Speed

0 = Switch OFF, 1 = Switch ON, X = Don't Care,
Min D = Minimum Duty Cycle,
Max D = Maximum Duty Cycle.

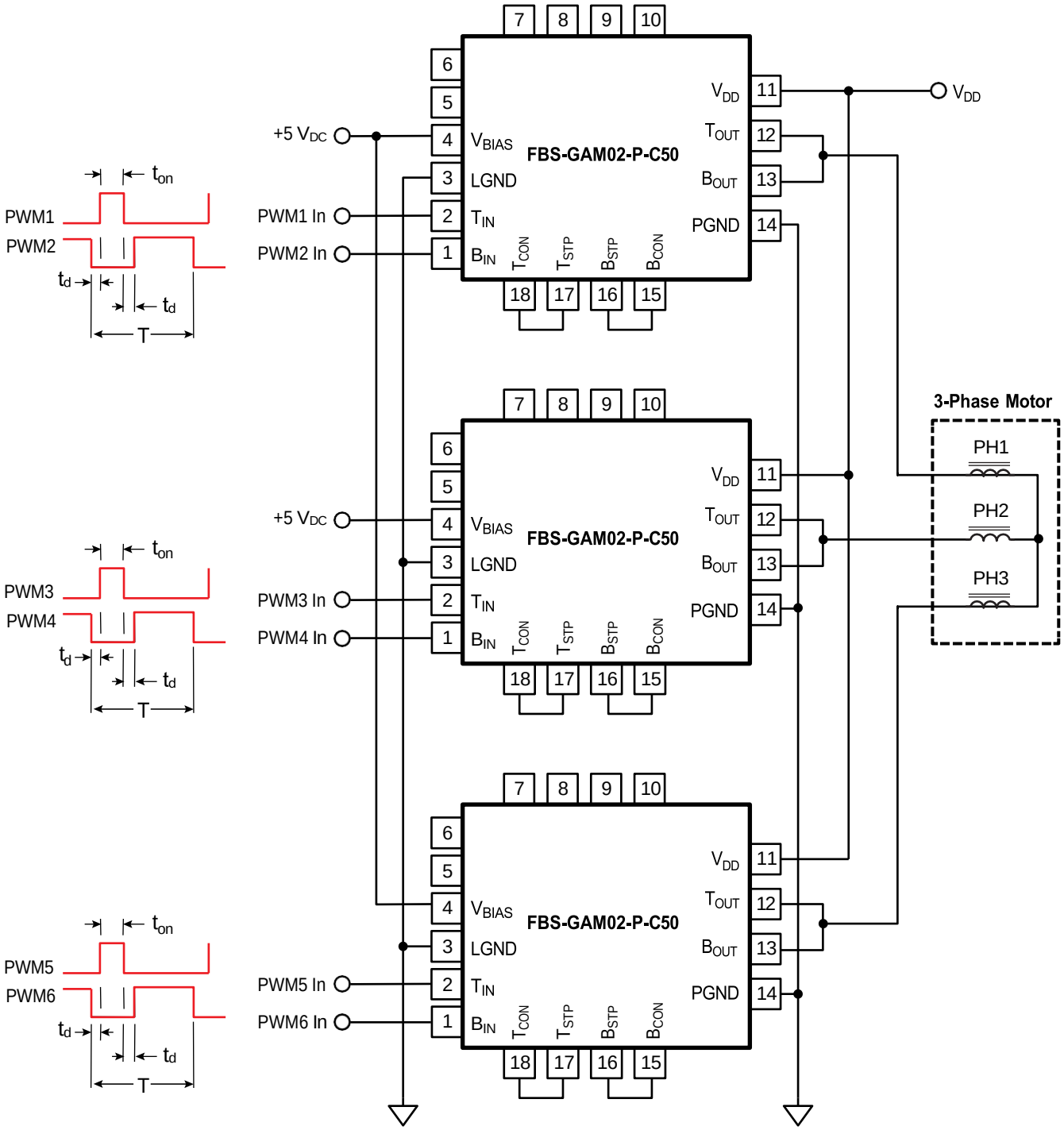


Figure 14. Half-Bridge Configuration: Three Phase Motor Drive Stage

Interfacing the FBS-GAM02 to Legacy Rad-Hard PWM Controllers

The B_{IN} and T_{IN} logic inputs for the FBS-GAM02-P-C50 have a desired maximum input voltage level limit of 5 V_{DC} due to the requirements of the eGaN HEMT technology utilized in the Module. This may seem to preclude the use of the GAM02 with legacy rad-hard PWM controllers such as the 182X family -- whose PWM outputs are 12 V_{DC}, minimum -- due to this logic input voltage limitation. But this is not the case as there are several ways to interface the GAM02 to these controllers:

a.) Zener diode voltage clamp with dead-time generation circuit

A Zener diode may be used to clamp the B_{IN} and T_{IN} logic inputs of the FBS-GAM02-P-C50 in order to interface the module to a high output voltage level PWM controller, as shown in Figure 15. The output of the UC1823A is a totem-pole configuration, and the output switches between 0 V_{DC} and 12 V_{DC} as logic 0 and logic 1, respectively. The transition times between logic states for a 1000 pF load are typically 20 ns, but much faster with lighter loads.

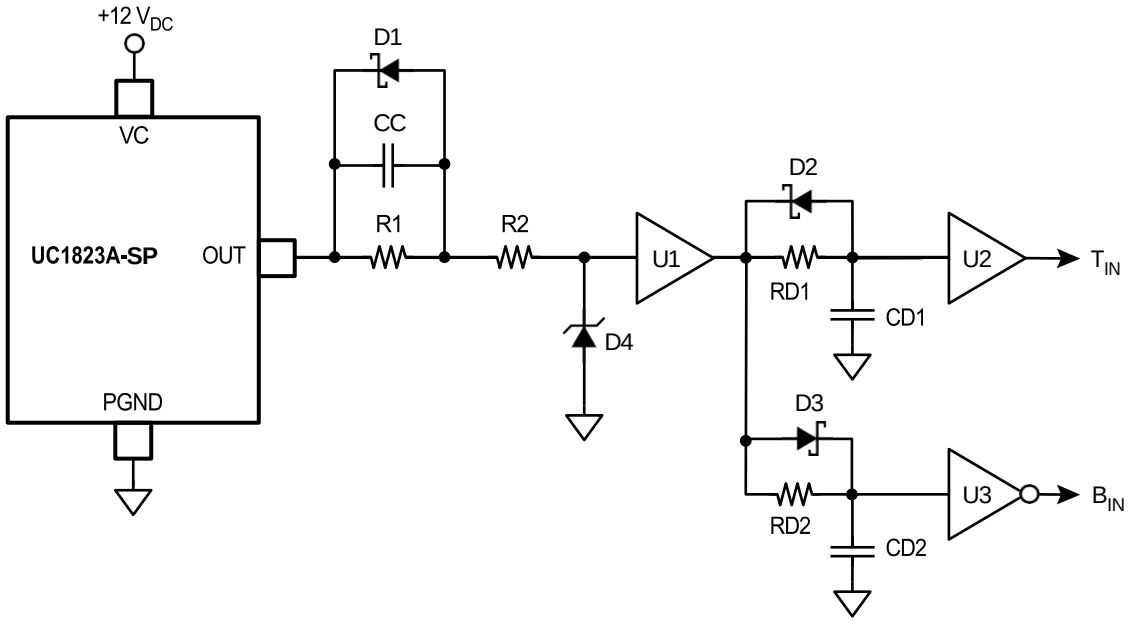


Figure 15. Zener Diode Logic Input Voltage Clamp Circuit and Dead Time Delay Circuit

The nominal voltage of the Zener diode, D4, should be 2.7 V_{DC} if U1 through U3 are 3.0 or 3.3 V_{DC} CMOS logic, and 4.3 V_{DC} if U1 though U3 are 5.0 V_{DC} CMOS logic. Depending upon the Zener diode chosen, the junction capacitance can be quite high – in the range of 250 to 500 pF. This is far greater than the typical input capacitance of the GAM02, which is 7 pF, and thus must be compensated for. Select capacitor CC, the speed-up capacitor, to achieve the fastest rise time at the input of U1. Select R1 to limit the minimum current through Zener D4 to be the nominal Zener current. Select R2 to limit the peak Zener current to less than the Zener peak current rating. Schottky diodes D1 through D3 are types RB751S40 or equivalent. Logic gates U1 and U2 are high-speed buffers, preferably with Schmitt-trigger inputs and logic gate U3 is a high-speed inverter, again preferably with Schmitt-trigger input. These three logic gates, along with resistors RD1 and RD2 and capacitors CD1 and CD2 form the dead-time circuit required for the GAM02 when it is connected in the half-bridge configuration, such as for the power output stage of a POL DC-DC converter. In the circuit, resistor RD1 and capacitor CD1 implement the time delay t_{d1} and RD2 and CD2 implement the time delay t_{d2} (see Notes 12 and 21). Set RD1 and RD2 to 1 kΩ and then select CD1 and CD2 to obtain time delays t_{D1} and t_{D2} as shown in the “Half-Bridge Configuration Dynamic Electrical Characteristics” parametric table on page 5. All component values and performance criteria should be verified with simulation modeling.

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Interfacing the FBS-GAM02 to Legacy Rad-Hard PWM Controllers *(continued)*

b.) Zener diode voltage clamp with ASIC/FPGA Two-Phase PWM Generator.

The same Zener diode clamping circuit as shown in Figure 15 may be used to clamp the output of the UC1823A to a lower voltage level in order to present it to an ASIC/FPGA in order to generate the requisite two-phase clock signals for the B_{IN} and T_{IN} logic inputs of the FBS-GAM02-P-C50. A typical circuit for this circuit implementation is shown in Figure 16:

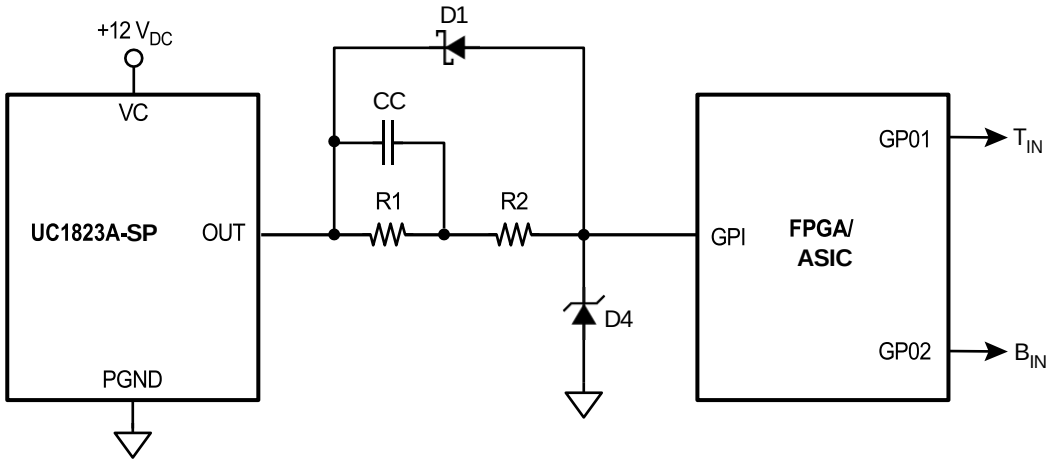

Figure 16. Zener Diode Logic Input Voltage Clamp Circuit with ASIC/FPGA Two-Phase Clock (With Dead Time) Generator

In the circuit of Figure 16 all the high-speed and high accuracy analog functions associated with the PWM controller are performed off-chip from the FPGA/ASIC. The programmable logic of the FPGA/ASIC and the associated firmware code is responsible for generating the two-phase clock with dead times required by the B_{IN} and T_{IN} inputs of the FBS-GAM02-P-C50.

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Adaptive Dead Time Control For the FBS-GAM02-P-C50

In circuits shown in both Figure 15 and 16 the dead times required by the FBS-GAM02-P-C50 to avoid cross-conduction/shoot-through are generated in a “brute force” manner either with analog components (Figure 15) or with programmable logic and firmware in an FPGA/ASIC (Figure 16). There is another way to obtain the optimum dead times for the FBS-GAM02-P-C50 device – adaptive dead time control, as shown in Figure 17.

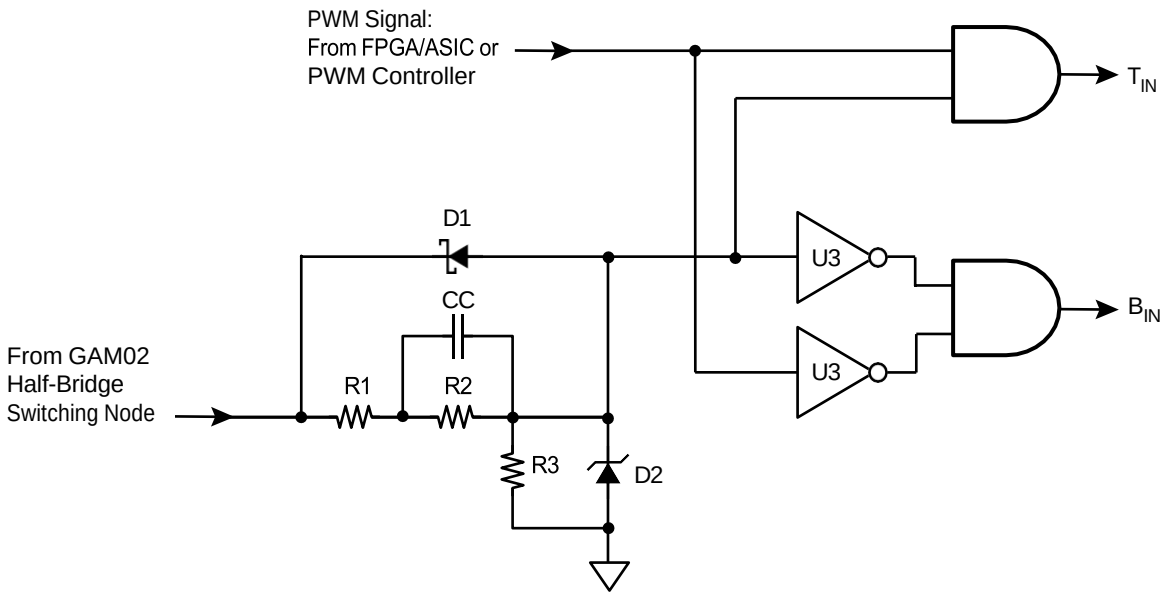

Figure 17. Adaptive Dead Time Control for Cross-Conduction/Shoot-Through Avoidance

Adaptive dead time control utilizes the state of the switching node (SN) of the GAM02 in order to allow the B_{IN} or T_{IN} signals (in this case the B_{IN} signal is the simple logical inverse of the T_{IN} signal) to be applied to the B_{IN} or T_{IN} logic inputs of the FBS-GAM02-P-C50 in order to avoid dynamic cross-conduction/shoot-though in the low- and high-side output power HEMTs. If the switching node of the FBS-GAM02-P-C50 is “low” (i.e. at PGND) then the low-side switch is turned ON, or in the process of turning OFF, and the high-side switch must not be turned ON (i.e. a logic 1 applied to the T_{IN} input). Similarly, if the switching node is “high” (i.e. at V_{DD}), then the-high side switch is turned ON, or in the process of turning OFF, and the low-side switch must not be turned ON (i.e. a logic 1 applied to the B_{IN} input). However, if the B_{IN} input is logic 0 and the switching node is “high” (i.e. the high-side catch Schottky conducting load current) then the T_{IN} input may be set to logic 1 to turn on the high-side driver. This same situation applies to the high-side driver: If the T_{IN} input is logic 0 and the switching node is “low” (i.e. the low-side catch Schottky is conducting load current) then the B_{IN} input may be set to logic 1 to turn on the low-side driver. The circuit shown in Figure 17 relies on a similar voltage clamping scheme for the switching node as was utilized in Figures 15 and 16, with the exception that the power supply V_{DD}, and subsequent range of the switching node, could be much higher than 12 V_{DC} – in fact up to 50 V_{DC} for the FBS-GAM02-P-C50. So greater care must be exercised in the selection of the clamping components to avoid excessive power dissipation in them, and the associated decrease in circuit efficiency. It is strongly recommended to simulate the circuit once the components have been selected to ensure that the proper clamping level is achieved and that the power dissipation of the clamp circuit is kept to a reasonable level so as not to affect overall circuit operating efficiency.

The key objective in the application of the adaptive dead time control circuit is to minimize the time delay associated with the voltage clamping circuit. Ideally, the desired time delay of the clamping circuit is zero in order to achieve the lowest (optimum) dead times. However, some delay is expected because the Zener diode clamp has finite capacitance and the biasing/current limiting delay resistors contribute an R1-C_{zener} inherent delay. There are certainly other methods to level-shift and monitor the switching node so as to ascertain its voltage level/state. Again, the key is to determine that state as quickly as possible so that switching decisions may be made at the B_{IN} and T_{IN} inputs of the FBS-GAM02-P-C50 as quickly as possible.

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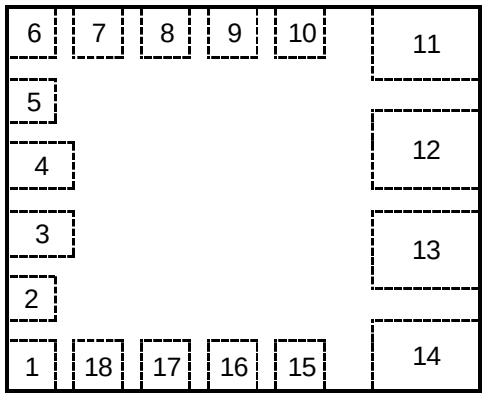
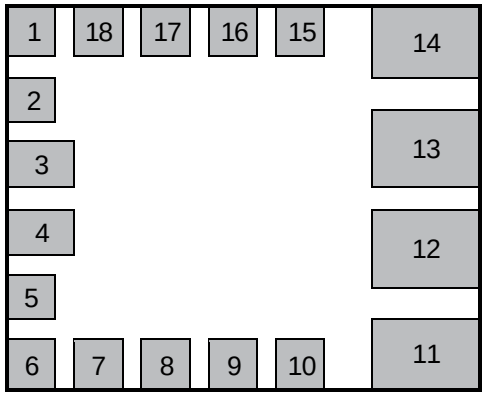
Pin Descriptions

18 Pin Molded SMT Package with Pillar Pins

Top (X-Ray) View



Bottom (Pad) View



B_{IN} (Pin 1)

The B_{IN} pin is the logic input for low-side power driver. When the B_{IN} input pin is logic low ("0"), the low-side output (B_{OUT}-PGND) pins (pins 13 and 14) are in the OFF (high-impedance) state. When the B_{IN} input pin is logic high ("1"), the B_{OUT}-PGND pins are in the ON (low impedance) state.

T_{IN} (Pin 2)

The T_{IN} pin is the logic input for high-side power driver. When the T_{IN} input pin is logic low ("0"), the high-side output (V_{DD}-T_{OUT}) pins (pins 11 and 12) are in the OFF (high impedance) state. When the T_{IN} input pin is logic high ("1"), the V_{DD}-T_{OUT} pins are in the ON (low impedance) state.

LGND (Logic Ground) (Pin 3)

For proper operation of the FBS-GAM02-P-C50, the LGND pin (Pin 3) MUST be connected directly to the system logic ground return in the application circuit.

V_{BIAS} (Pin 4)

The V_{BIAS} pin is the raw input DC power input for the FBS-GAM02-P-C50 module. It is recommended that a 1.0 microfarad ceramic capacitor and a 0.1 microfarad ceramic capacitor, each 25 V_{DC} rating, be connected between V_{BIAS} (pin 4) and system power ground plane (the common tie point of PGND1 and the ground plane) to obtain the specified switching performance.

PG (Power Good) (Pin 5)

The PG pin is an open drain logic-compatible output. For proper operation the PG pin must be pulled-up to V_{BIAS}, external to the module, with a 4.7 kΩ resistor.

The FBS-GAM02-P-C50 incorporates a Power Good (PG) sensing circuit that disables both the low- and high-side internal gate drivers when the +5 V_{DC} gate drive bias potential (V_{BIAS}) falls below an under-voltage threshold, typically 4.45 V_{DC}, or rises above a potentially- damaging V_{BIAS} over-voltage threshold level – refer to Figure 5 for the proper operational nomenclature and functionality versus the state of the V_{BIAS} power supply. During the time when the V_{BIAS} potential is outside of the pre-set threshold(s), the PG output (Pin 5) pin is logic low ("0"). Alternatively, when the V_{BIAS} potential is within the pre-set thresholds the PG pin is logic high ("1"). The logic condition of the PG pin may be sensed by a rad hard FPGA or Microcontroller/DSP in-order to determine when the power switches in the FBS-GAM02-P-C50 may be driven with a pulse-width modulated (PWM) input signal(s) at the B_{IN} and T_{IN} logic inputs. If either the under-voltage and over-voltage indication features are not required or desired, then these functions may be disabled separately by connecting the *SD (Pin 6) pin to V_{BIAS} (pin 4) for the UVLO or the SD pin (Pin 7) to LGND (pin 3) for the 0 V_{DC} indicator, as shown in Figure 18.

***SD (Pin 6)**

The *SD pin is a low-true disable input for the FBS-GAM02-P-C50 module.

Both the low- and high-side power switches may be disabled (set to their high impedance OFF state) utilizing the *SD input, as shown in Figure 20. To disable the FBS-GAM02-P-C50 module power outputs, the *SD (Pin 6) input may be driven by an open drain or open collector that pulls this input to logic ground (LGND, pin 3). If the *SD shutdown function is not required, this pin should be left OPEN (no connection).

SD (Shutdown) (Pin 7)

The SD pin is a high-true disable input for the FBS-GAM02-P-C50 module.

Both the low- and high-side power switches may be disabled (set to their high impedance OFF state) utilizing the SD input, as shown in Figure 21. To disable the FBS-GAM02-P-C50 module power outputs, the SD (Pin 7) input may be driven by an open drain or open collector that pulls this input to V_{BIAS} (pin 4). If the SD shutdown function is not required, this pin should be left OPEN (no connection).

TOS (Pin 8)

The TOS pin is the external connection to the switching node side (T_{OUT}) of the high-side gate driver internal bootstrap capacitor.
If additional, external, bootstrap capacitance is desired, then this capacitor should be connected between TOS and TBST (pin 10).
If external bootstrap capacitance is required, then pin 8 should be left OPEN (no connection).

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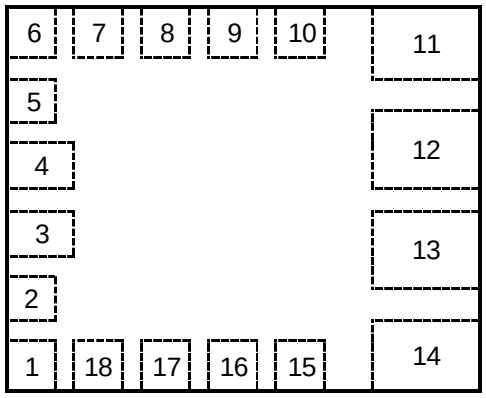
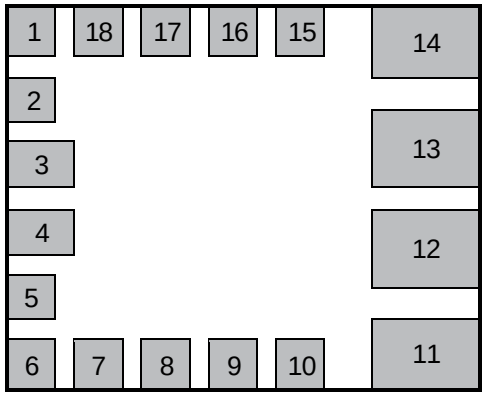
Pin Descriptions *(continued)*

18 Pin Molded SMT Package with Pillar Pins

Top (X-Ray) View



Bottom (Pad) View



N/C (Pin 9)

Pins 9 is not internally connected. This "no connection" pin is recommended to be connected to the system PGND (plane) as good engineering practice to avoid coupling unwanted noise into the internal circuitry of the FBS-GAM02-P-C50. This may be done directly or using a 0 Ω jumper resistor.

TBST (Pin 10)

The TBST pin is connected directly to the bias side (the bootstrap diode cathode connection) of the internal bootstrap capacitor for the high-side gate driver. The TBST, in conjunction with the TOS pin, provides the end-user the ability to add additional external bootstrap capacitance to the high-side gate driver to allow the FBS-GAM02-P-C50 to be operated at lower switching frequencies (< 200kHz) than specified in this data-sheet. An external isolated power supply may be provided to Pins 8 (-) and 10 (+) to achieve DC operation of the high-side switch, only if great care is used in the design of this supply to insure that it may withstand the very high dV/dt signal present at Pins 8 and 10.

If external bootstrap capacitance is required, then pin 10 should be left OPEN (no connection).

VDD (Pin 11)

The V_{DD} pin (pin 11) is the high current reference (open drain) pin for the internal power eGaN® HEMT associated with high-side power driver. This pin should be connected directly to the system power (V_{DD}) bus via a low impedance connection, preferably through a low impedance power plane. This pin should be properly bypassed to the system power ground (PGND) using the guidelines found in the "*Recommended V_{DD}-to-PGND Power Supply Bypassing*" section, following.

T_{OUT} (Pin 12)

The T_{OUT} pin (pin 12) is the high-current output pin for the high-side driver in the FBS-GAM02-P-C50 module. This pin should be connected directly, via a low impedance connection, to the external load in high-side switch applications or to the B_{OUT} pin (pin 11), and the load, in half-bridge configurations. The internal high-side gate driver circuitry is referenced to the T_{OUT} pin, which is internally connected to the TOS pin (pin 8).

This is a VERY high dV/dt and dI/dt pin and regardless of the switch configuration the connection to the external load should be as short as possible to minimize radiated EMI.

B_{OUT} (Pin 13)

The B_{OUT} pin (pin 13) is the high current output (open drain) pin for the internal power eGaN® HEMT associated with the low-side power driver. This pin should be connected directly, via a low impedance connection, to the external load in low-side switch applications or to the T_{OUT} pin (pin 12), and the load, in half-bridge configurations.

This is a VERY high dV/dt and dI/dt pin and the connection to the external load should be as short as possible to minimize radiated EMI.

PGND (Pin 14)

The PGND pin (pin 14) is the ground return (source) connection for the internal power circuitry eGaN® HEMT and high-speed gate driver circuitry associated with low-side power driver and for the power good and interface logic for the high-side driver. This pin should be connected directly to the system power return/ground plane to minimize common source inductance, and the voltage transients associated with this inductance. If load current sensing is required in the half-bridge configuration, this should be accomplished via a current sense transformer in series with the drain of the low-side power HEMT (pin 13).

B_{CON} (Pin 15)

The B_{CON} pin is the logic input for the input shoot-through protection for low-side power driver. The state of this pin follows the state of the T_{IN} logic input pin. If input shoot-through protection is desired in the half-bridge configuration where both power drivers (low and high) must not be turned on simultaneously if the B_{IN} and T_{IN} logic inputs are simultaneously at logic "1", then B_{CON} (pin 15) should be externally connected to B_{STP} (pin 16). If no shoot-through protection is desired, then pin 15 should be left OPEN (no connection).

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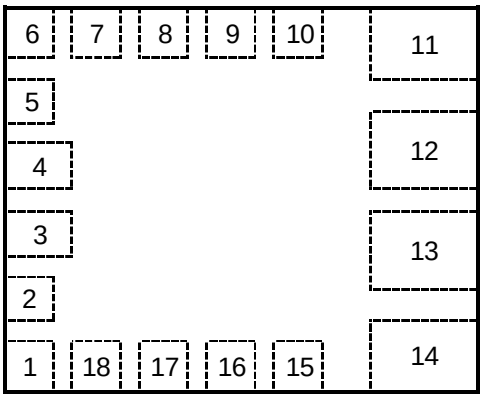
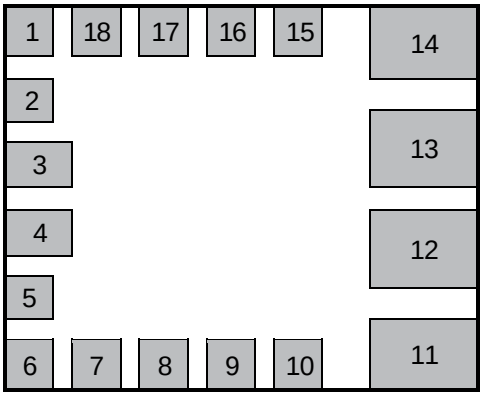
Pin Descriptions *(continued)*

18 Pin Molded SMT Package with Pillar Pins

Top (X-Ray) View



Bottom (Pad) View



B_{STP} (Pin 16)

The B_{STP} pin is the open drain output for the input shoot-through protection for low-side power driver. The state of this pin is the logical inverse of the B_{IN} logic input pin. If input shoot-through protection is desired in the half-bridge configuration where both power drivers (low and high) must not be turned on simultaneously if the B_{IN} and T_{IN} logic inputs are simultaneously at logic "1", then B_{STP} (pin 16) should be externally connected to B_{CON} (pin 15). If no shoot-through protection is desired, then pin 16 should be left OPEN (no connection).

T_{STP} (Pin 17)

The T_{STP} pin is the open drain output for the input shoot-through protection for high-side power driver. The state of this pin is the logical inverse of the T_{IN} logic input pin. If input shoot-through protection is desired in the half-bridge configuration where both power drivers (low and high) must not be turned on simultaneously if the B_{IN} and T_{IN} logic inputs are simultaneously at logic "1", then T_{STP} (pin 17) should be externally connected to T_{CON} (pin 18). If no shoot-through protection is desired, then pin 17 should be left OPEN (no connection).

T_{CON} (Pin 18)

The T_{CON} pin is the logic input for the input shoot-through protection for high-side power driver. The state of this pin follows the state of the B_{IN} logic input pin. If input shoot-through protection is desired in the half-bridge configuration where both power drivers (low and high) must not be turned on simultaneously if the B_{IN} and T_{IN} logic inputs are simultaneously at logic "1", then T_{CON} (pin 18) should be externally connected to T_{STP} (pin 17). If no shoot-through protection is desired, then pin 18 should be left OPEN (no connection).

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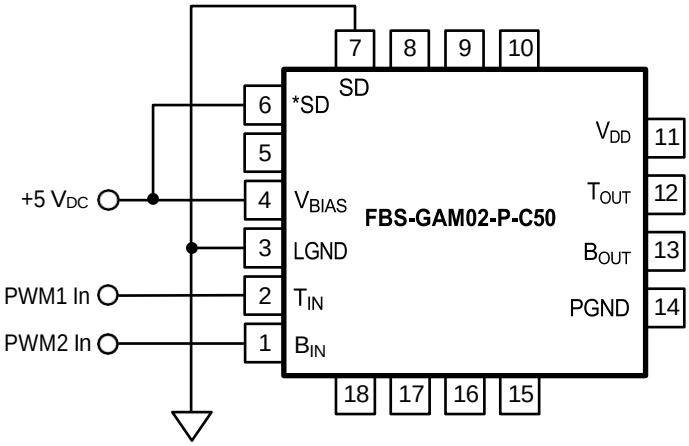

Figure 18. PG Protection Functions Disabled

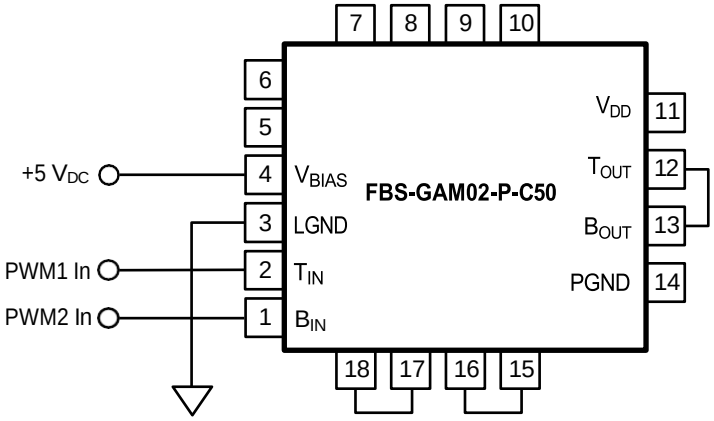

Figure 19. Shoot-Through Protection Function Enabled

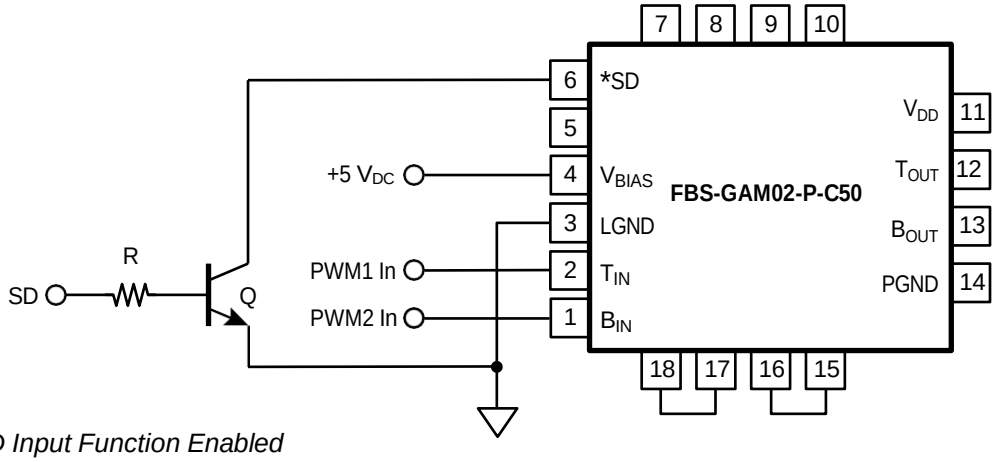

*Figure 20. *SD Input Function Enabled*

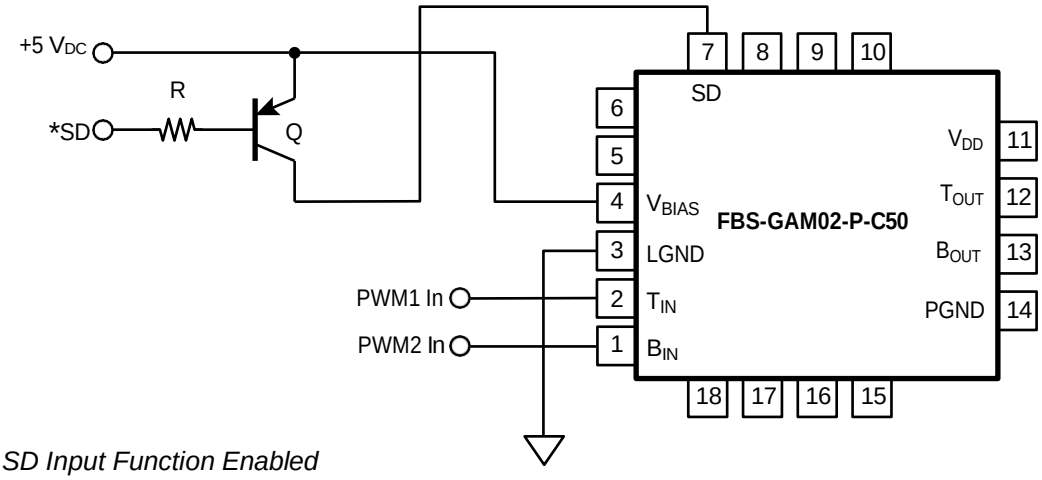

Figure 21. SD Input Function Enabled

High-Side Bootstrap Capacitor Periodic Recharge

The high-side power switch gate driver utilizes a bootstrap capacitor to provide the proper bias for this circuit during switching operation. As such, this capacitor **MUST** be periodically re-charged from the V_{BIAS} power supply. As a stand-alone high-side switch with a ground-connected/ground-sensed load, this recharging takes place each time the switch is turned OFF and the T_{OUT} node returns to ground potential (0 V_{DC}). However, when connected in conjunction with the low-side power switch in the Half-Bridge configuration (See Figure 11, for example), this connection to ground does not exist until the low-side power switch is turned ON, thus creating a low impedance connection from T_{OUT} through the low-side power switch (B_{OUT}-PGND). If the high-side gate driver is not provided with periodic recharge during operation, damage may occur to the Module.

The time t_{prg} is the minimum time required for the low-side driver to be turned ON in order to ensure that the bootstrap capacitor is properly charged when power is initially applied to the FBS-GAM02-P-C50 Module.

If DC operation is desired for the Module when connected as two single, independent, power drivers (see Figures 7, 8 or 9, for examples) then an isolated +4.5 to +5.5 V_{DC} power supply capable of operation with high rates-of-change of voltage from primary-to-secondary should be connected to the TBST (pin 10) and TOS (pin 9) pins on the Module to provide DC power to the high-side gate driver.

DC Operation and Power-Up Sequencing

The recommended power sequencing for the FBS-GAM02-P-C50 is the V_{BIAS} power supply is applied first and within the recommended operating voltage range prior to the application of V_{DD} to the circuit.

The FBS-GAM02P-R-50 is designed as a switching eGAN® HEMT multifunction driver that is inherently capable of DC (steady-state) operation. As such, there are precautions that must be observed during the application and operation of this Module. **One of these precautions is power-up sequencing. The power MUST be sequenced to the circuit with V_{BIAS} being applied first and within its recommended operating voltage range before V_{DD} is applied to the circuit. This will prevent the gate driver output (OUT) from assuming a non-deterministic state with regards to the logic input (IN) and unintentionally providing an internal drive signal to the internal eGaN® HEMT power switches. Under NO circumstances should an FBS-GAM02-P-C50 Module be used in a half-bridge configuration with V_{DD} applied first, prior to V_{BIAS}, to the Module.**

Recommended V_{DD}-to-PGND Power Supply Bypassing

The power supply pins and return pin of the FBS-GAM02-P-C50 require proper high frequency bypassing to one-another in order to prevent harmful switching noise-related spikes from degrading or damaging the internal circuitry in the FBS-GAM02-P-C50 module. The more critical bypassing situation is related to the V_{DD} supply to PGND (Pin 14), which bears the high rate-of-change voltages and currents associated with the internal eGaN® power switches interacting with a load. It is recommended that a minimum of two (2) 4.7 microfarad ceramic capacitors, one (1) 1.0 microfarad ceramic capacitor and one (1) 0.1 microfarad ceramic capacitor, all with 100 V_{DC} ratings, be connected from V_{DD} to PGND. All four of these capacitors should be low ESR types, if possible. It is strongly recommended that these capacitors inscribe the smallest possible loop area between V_{DD} and PGND so as to minimize the inductance related to this loop area. Figure 22 illustrates three instances of recommended and acceptable V_{DD}-PGND bypassing, as implemented in PCB copper etch. Regardless, different end-use implementations will require different V_{DD} bypass capacitor placements, and it is strongly recommended that the chosen bypassing scheme be evaluated in hardware for its effectiveness.

It is also recommended that a 1.0 microfarad ceramic capacitor and a 0.1 microfarad ceramic capacitor, each 25 V_{DC} rating, be connected between V_{BIAS} (pin 4) and PGND (pin 3).

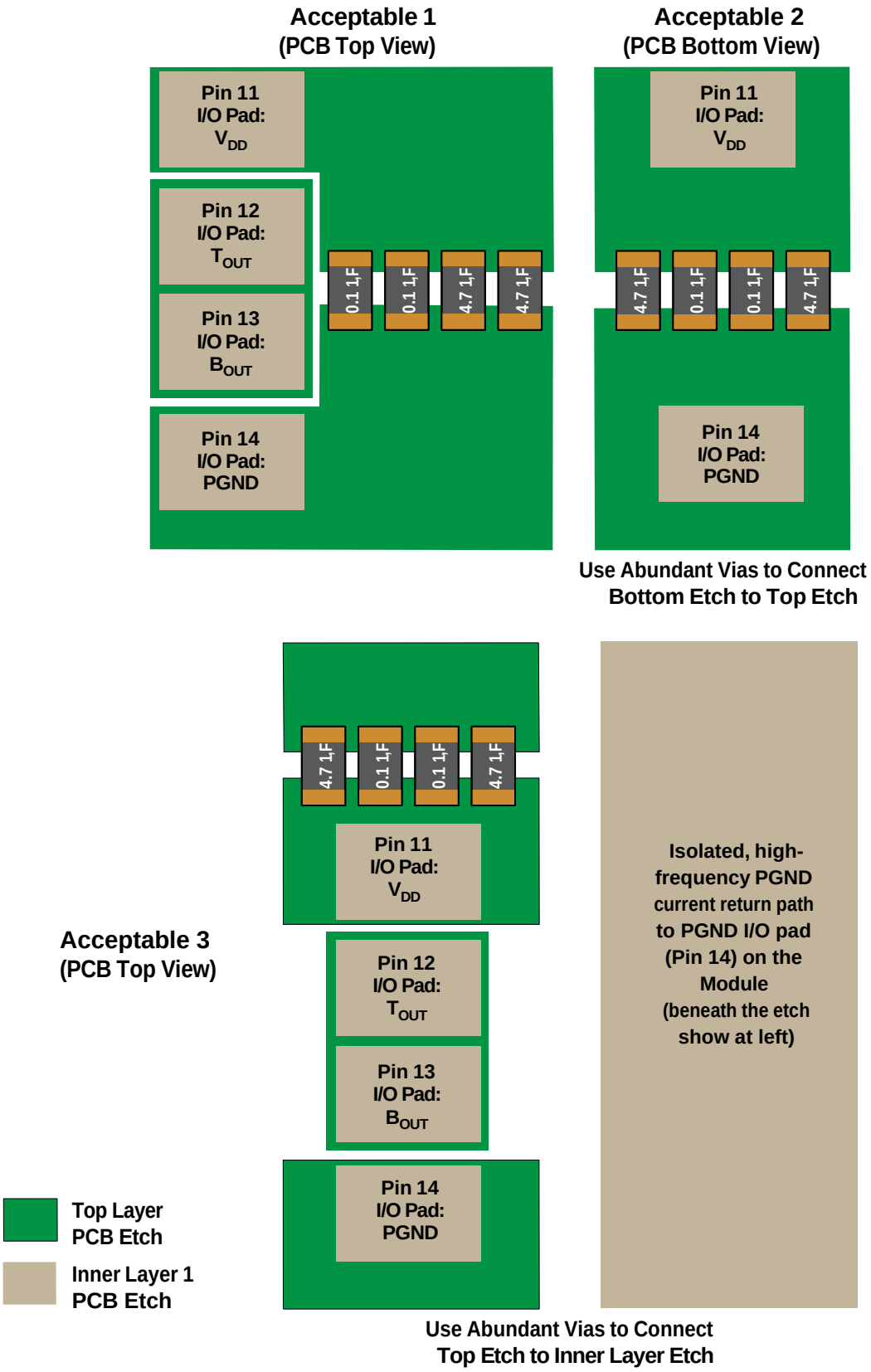

Figure 22. Recommended V_{DD}-to-PGND Power Supply Bypassing (Not to Scale)

Suggested FBS-GAM02-P-C50 Schematic Symbol

The suggested schematic symbol for the FBS-GAM02-P-C50 is shown in Figure 23. This symbol groups the I/O pins of the FBS-GAM02-P-C50 into groups of similar functionality.

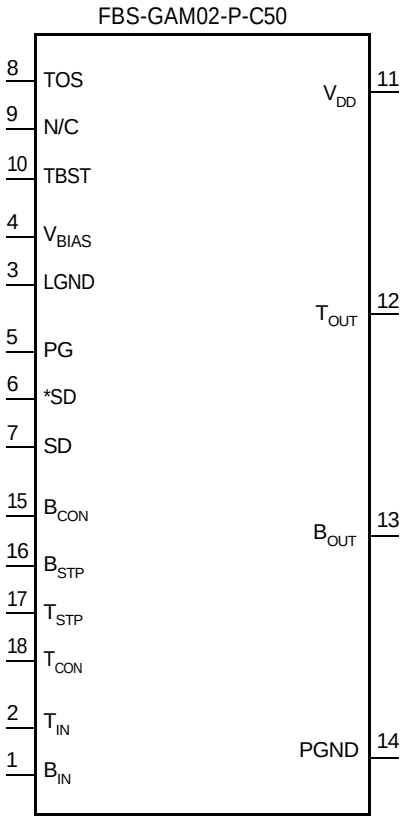

Figure 23. Suggested FBS-GAM02-P-C50 Schematic Symbol

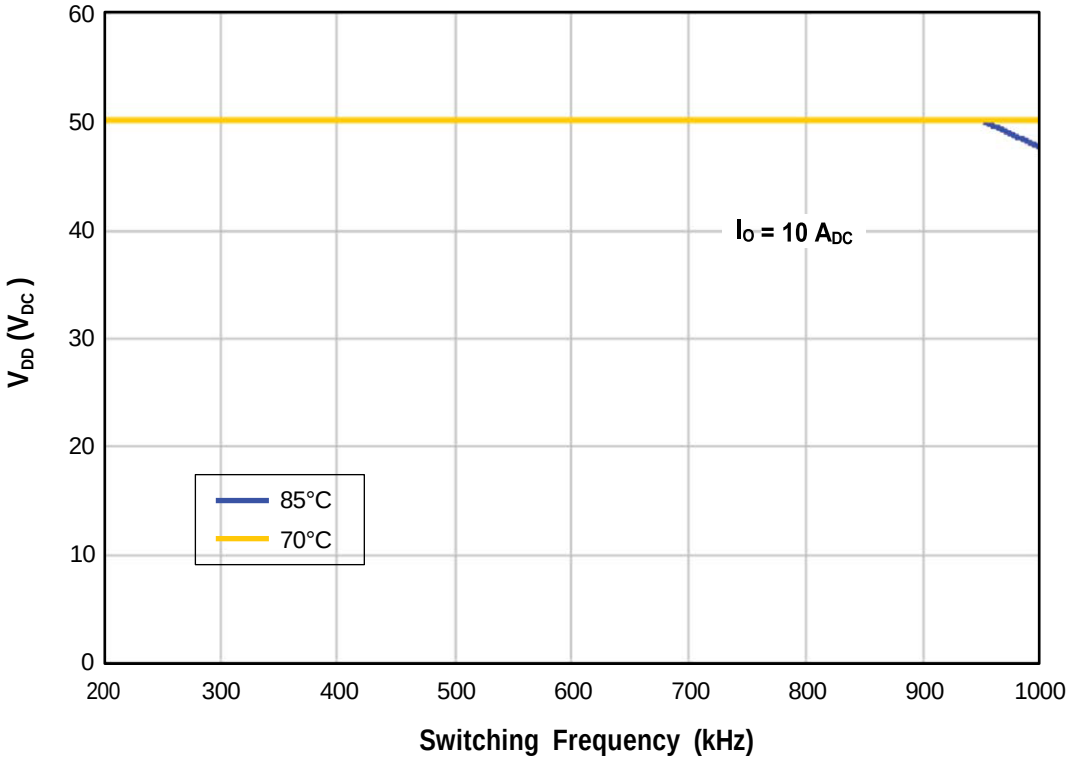

Figure 24. Maximum Switching Frequency vs. Supply Voltage (V_{DD}) vs. Module Case Temperature (T_c), I_o = 10 A, Half-Bridge Configuration.

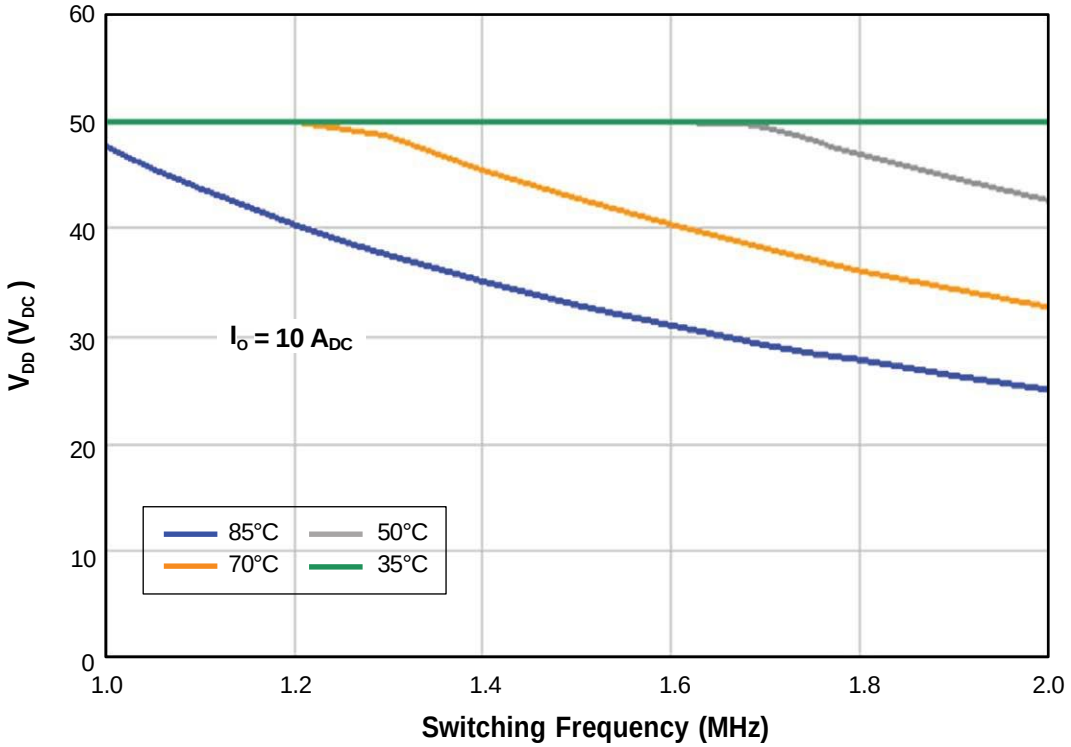

Figure 25. Maximum Switching Frequency vs. Supply Voltage (V_{DD}) vs. Module Case Temperature (T_c), I_o = 10 A, Half-Bridge Configuration.

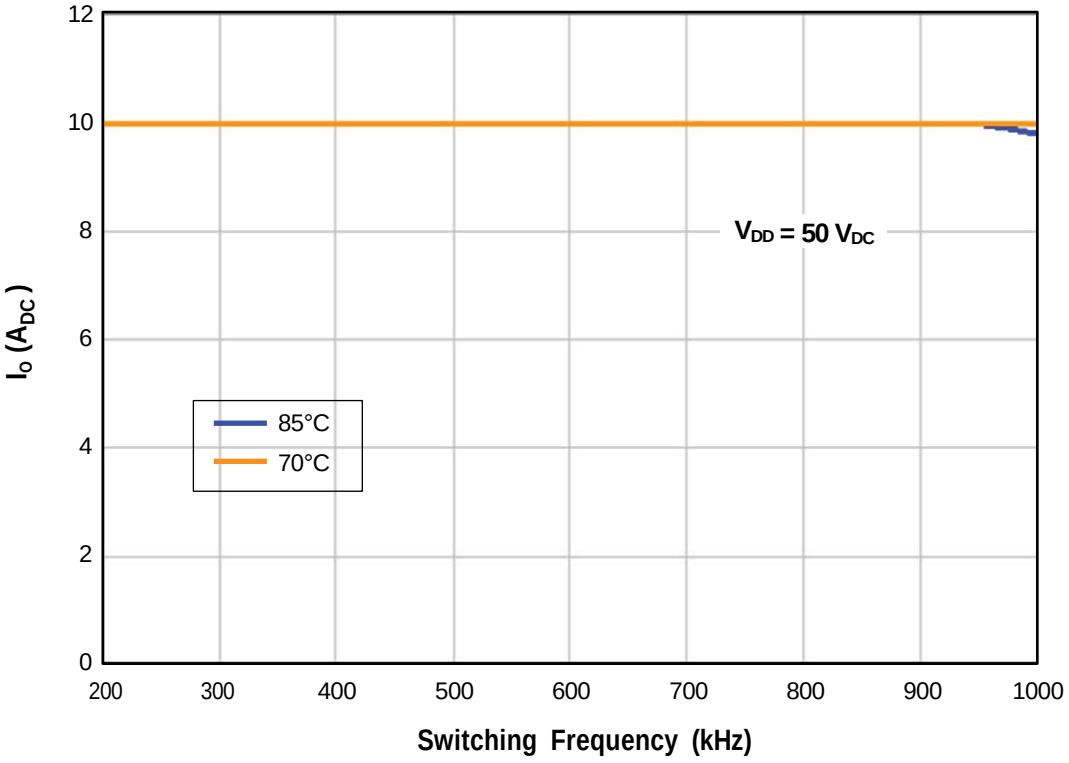

Figure 26. Maximum Output Current (I_o) vs. Switching Frequency (f_{sw}) vs. Module Case Temperature (T_c), V_{DD}= 50 V_{DC}, Half-Bridge Configuration.

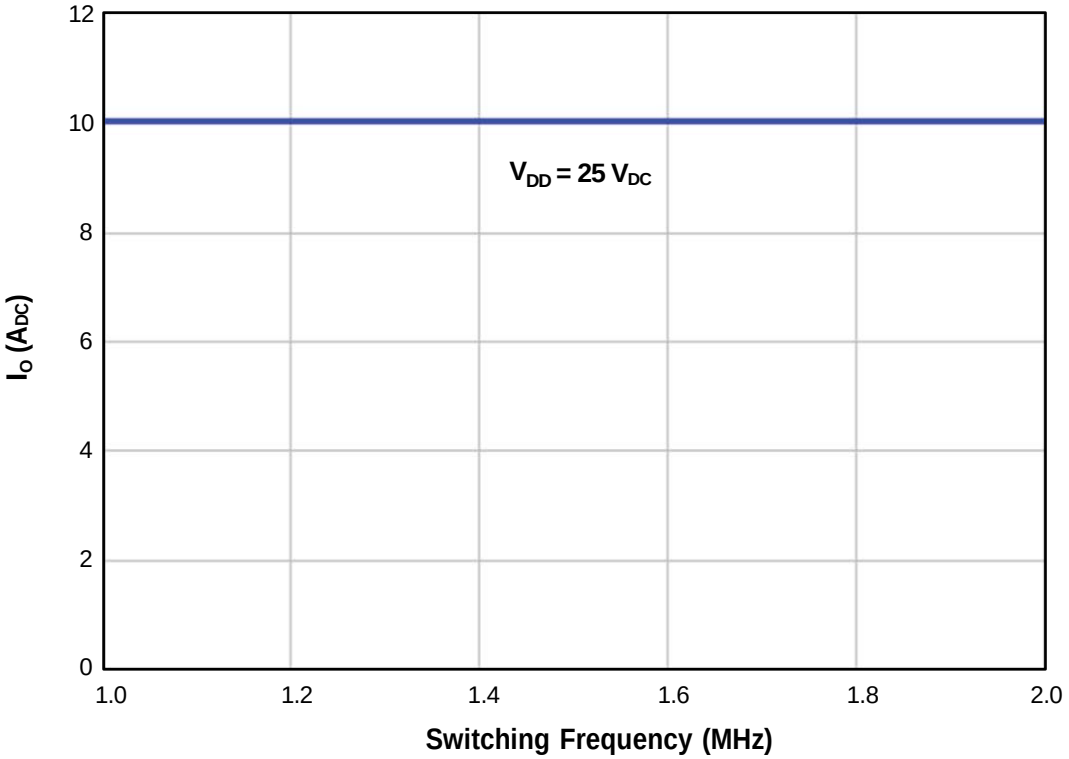

Figure 27. Maximum Output Current (I_o) vs. Switching Frequency (f_{sw}) vs. Module Case Temperature (T_c), V_{DD} = 25 V_{DC}, Half-Bridge Configuration.

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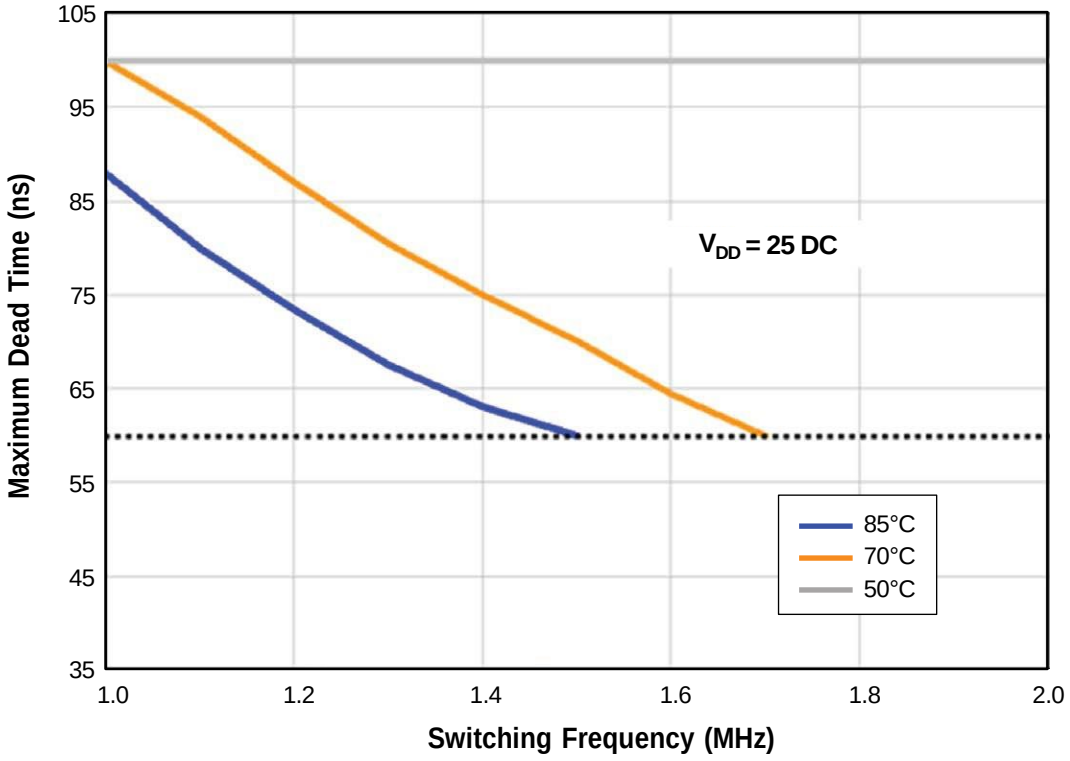

Figure 28. Maximum Dead Time (t_{dt}) vs. Switching Frequency (f_{sw}) vs. Module Case Temperature (T_c), V_{DD} = 25 V_{DC}, Half-Bridge Configuration (Refer to Fig. 23).

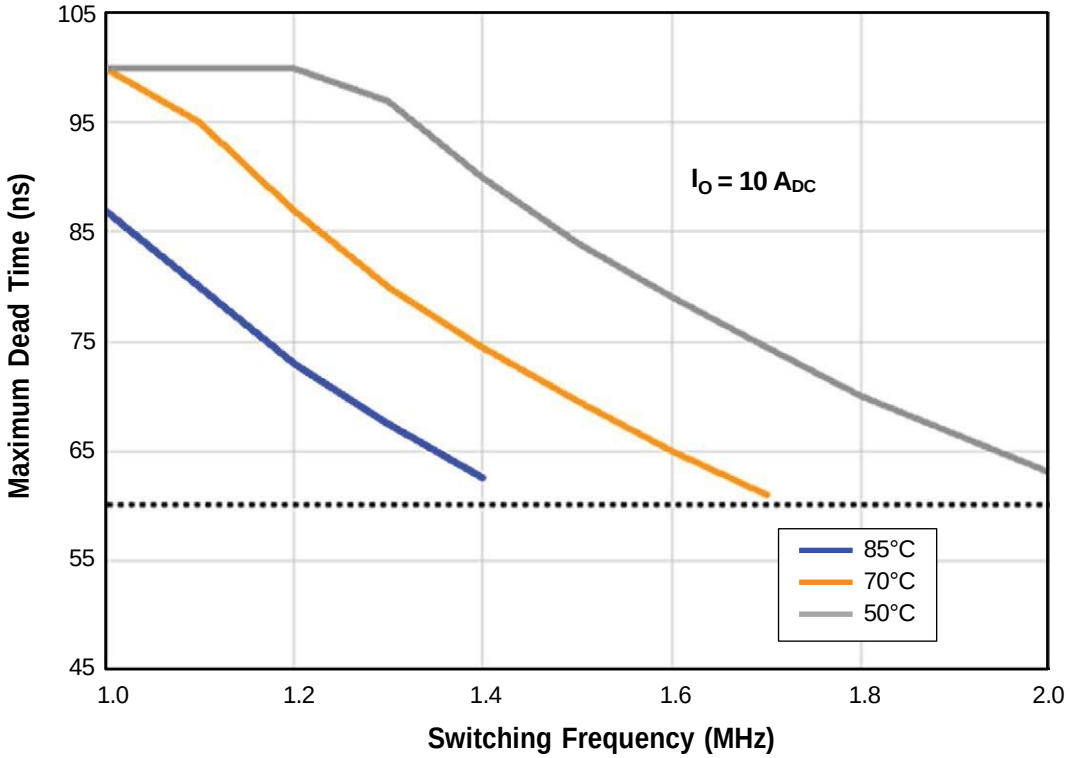

Figure 29. Maximum Dead Time (t_{dt}) vs. Switching Frequency (f_{sw}) vs. Module Case Temperature (T_c), I_o = 10 A, Half-Bridge Configuration (Refer to Fig. 21).

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Thermal Characteristics

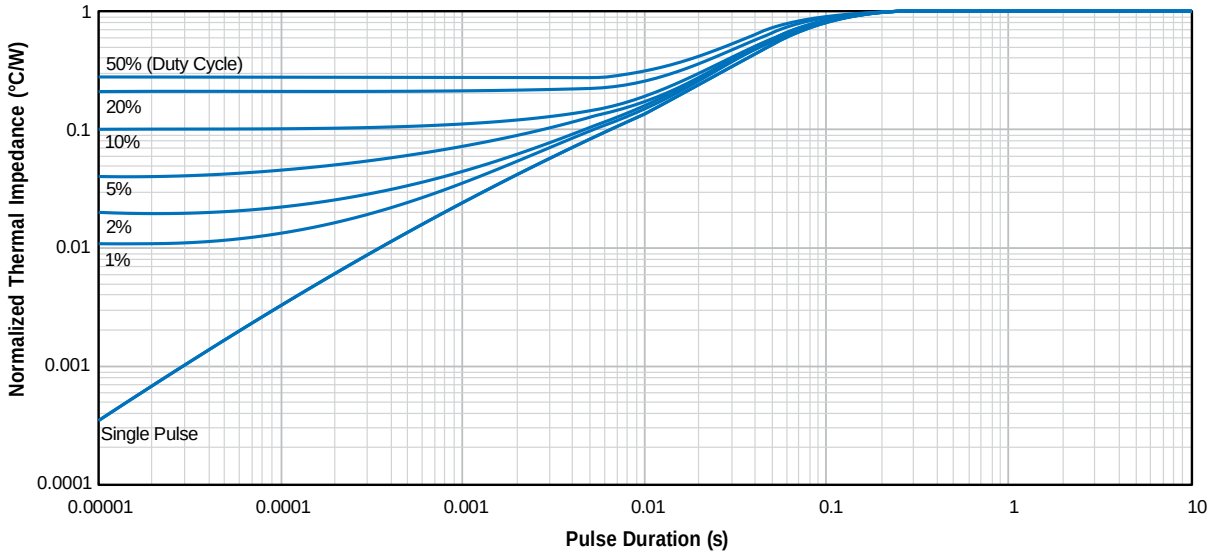


Figure 30. Typical Low- or High-Side Power eGAN® HEMT Normalized Junction-to-Case Thermal Impedance

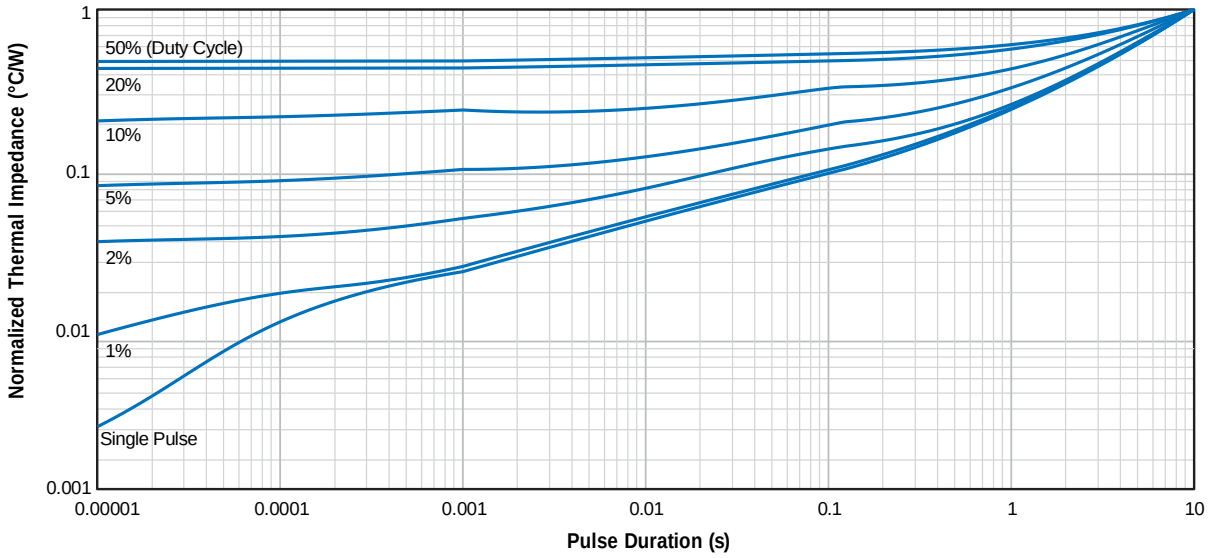
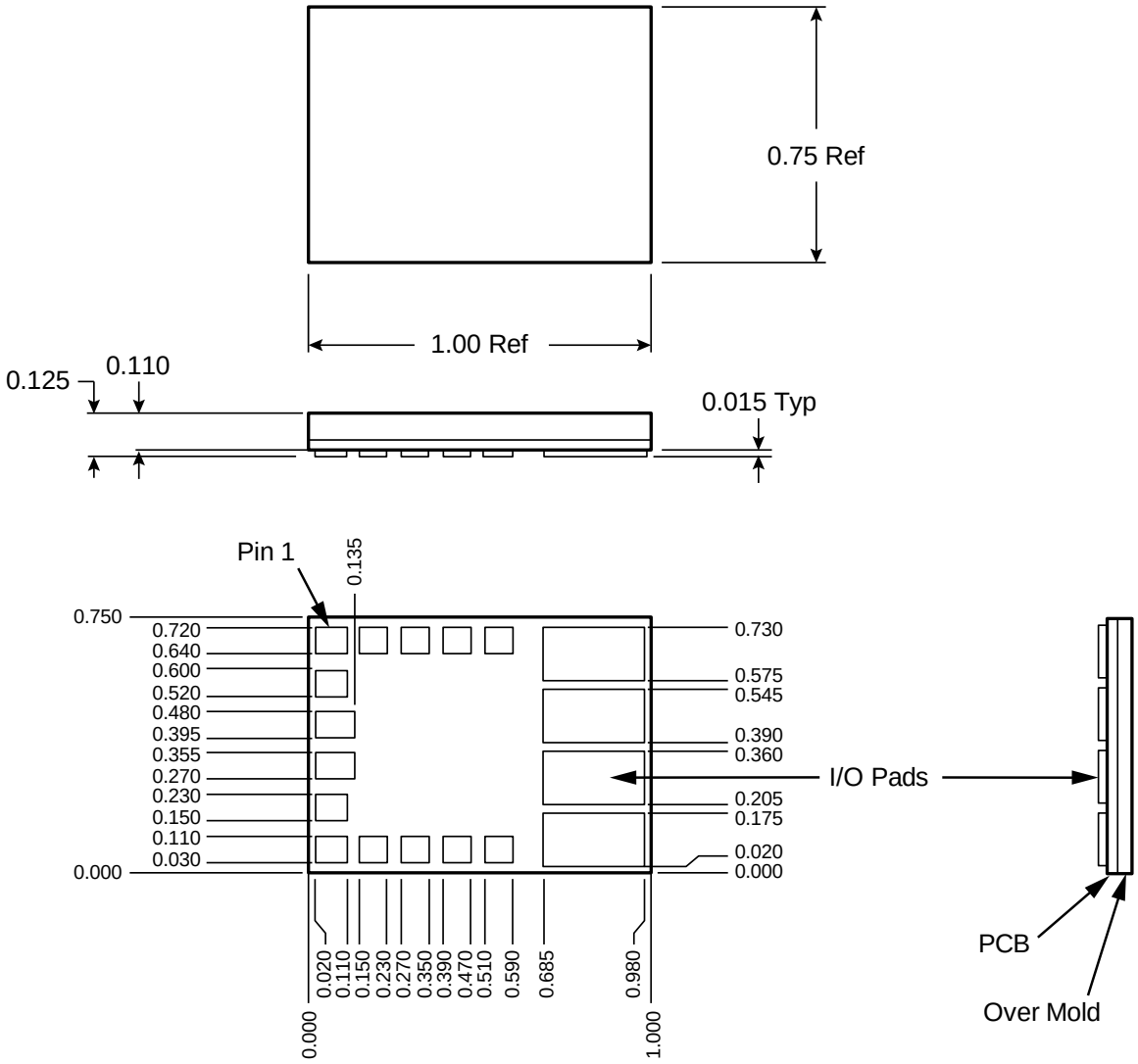


Figure 31. Typical Low- or High-Side Catch Schottky Normalized Junction-to-Case Thermal Impedance

Package Outline and Dimensions



Note: All dimensions are in inches
ALL tolerances +/- 0.010

Figure 32. FBS-GAM02-P-C50 Package Outline and Dimensions

Recommended PCB Solder Pad Configuration

The novel I/O "pillar" pads fabricated onto the pad-side surface of the FBS-GAM02-P-C50 module are designed to provide optimal electrical, thermal and mechanical properties for the end-use system designer. To achieve the full benefit of these properties, it is important that the FBS-GAM02-P-C50 module be soldered to the PCB motherboard using SN63 (or equivalent) solder. Care should be taken during processing to insure there is minimal solder voiding in the contacts to the V_{DD} (pin 11), T_{OUT} (pin 12), B_{OUT} (pin 13) and PGND (Pin 14) pads on the module. The recommended pad dimensions and locations are shown in Figure 33. All dimensions are shown in inches.

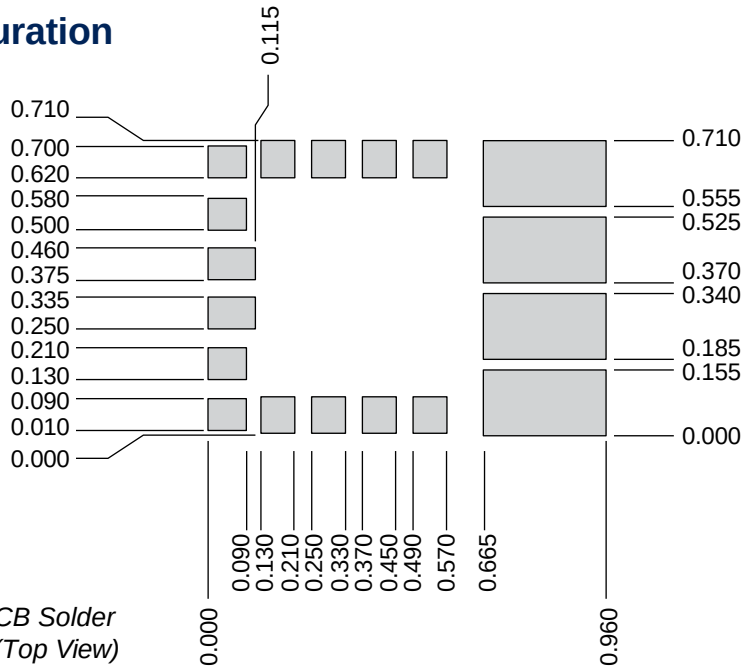


Figure 33. Recommended PCB Solder Pad Configuration (Top View)

Sn63/Pb37 No Clean Solder Paste Typical Example Profile

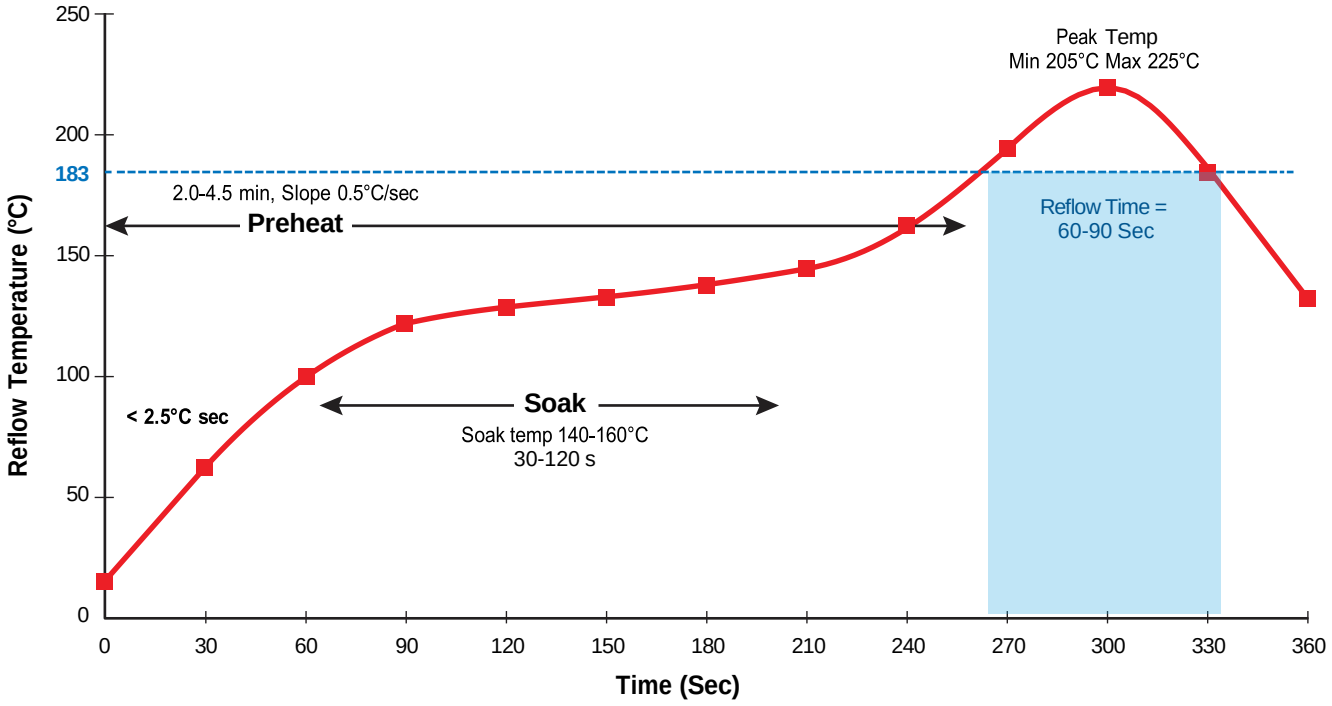


Figure 34. Sn63/Pb37 No Clean Solder Paste Typical Reflow Example Profile.

Preheat Zone – The preheat zone, is also referred to as the ramp zone, and is used to elevate the temperature of the PCB to the desired soak temperature. In the preheat zone the temperature of the PCB is constantly rising, at a rate that should not exceed 2.5°C/sec. The oven's preheat zone should normally occupy 25-33% of the total heated tunnel length.

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The Soak Zone – normally occupies 33-50% of the total heated tunnel length exposes the PCB to a relatively steady temperature that will allow the components of different mass to be uniform in temperature. The soak zone also allows the flux to concentrate and the volatiles to escape from the paste.

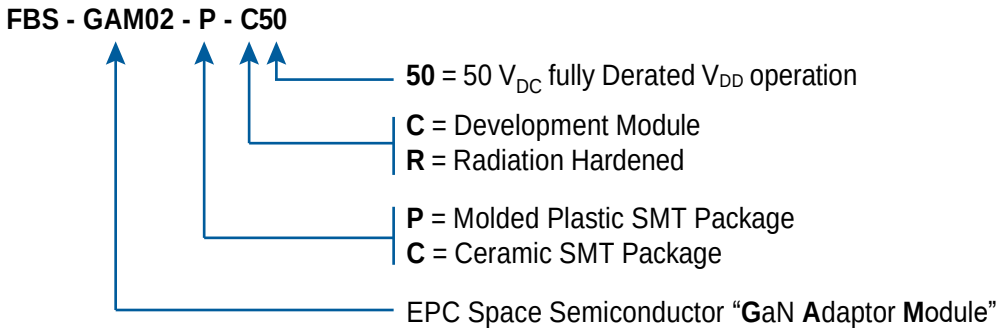
The Reflow Zone – or spike zone is to elevate the temperature of the PCB assembly from the activation temperature to the recommended peak temperature. The activation temperature is always somewhat below the melting point of the alloy, while the peak temperature is always above the melting point.

Reflow – Best results achieved when reflowed in a ***forced air convection*** oven with a minimum of 8 zones (top & bottom), however reflow is possible with a four (4)-zone oven (top & bottom) with the recommended profile for a forced air convection reflow process. The melting temperature of the solder, the heat resistance of the components, and the characteristics of the PCB (i.e. density, thickness, etc.) determine the actual reflow profile. **Note* FBS-GAM02-P-C50 solder attachment has a maximum peak dwell temperature of 230°C limit, exceeding the maximum peak temperature can cause damage to the unit.**

Reflow Process Disclaimer

The profile is as stated "Example". The-end user can optimize reflow profiling based against the actual solder paste and reflow oven used. EPC Space assumes no liability in conjunction with the use of this profile information.

EPC Space Part Number Information



*FBS-GAM02-P-C50 (May or May not utilize High Lead Content Die) and
FBS-GAM02-P-R50 (Utilizes High Lead Content Die)

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